MAGNETIC PERIPHERALS INC.
a subsidiary of CONTROL DATA CORPORATION

ENGINEERING SPECIFICATION

NORMANDALE OPERATIONS

SPEC 64712400
CD 7
REV K
DATE 03/27/81

0010A 0015S

FLAT CABLE

INTERFACE SPECIFICATION

FOR

THE SMD, MMD, FHT MMD, FMD, LMD, AND CMD FAMILIES

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

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NRMOPS DISK DRIVE DEVELOPMENT		B. C. [illegible]	[illegible]	
NRMOPS CIRCUIT DESIGN		X	X	X
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AA1836 1/77

TABLE OF CONTENTS

ILLUSTRATIONS

Figures

Tables

1.0 SCOPE

This document describes the interface requirements of the Magnetic Peripherals Inc. SMD, MMD, FHT MMD, CMD, LMD, and FMD type disk drives.

2.0 APPLICABLE DOCUMENTS

SPEC 64709300 - Product Specification Storage Module Drive (SMD)
SPEC 64709700 - Product Specification Mini-Module Drive (MMD)
SPEC 75888221 - Product Specification Cartridge Module Drive (CMD)
SPEC 64713400 - Product Specification Fixed Head Per Track Mini-Module Drive (FHT MMD)
SPEC 64713600 - Product Specification 9775 Fixed Module Drive (FMD)
SPEC 77641922 - Product Specification for 9455 Lark Module Drive (LMD)

3.0 GENERAL DESCRIPTION

The interface for all SMD, MMD, FHT MMD, CMD, LMD, and FMD devices use compatible line drivers and receivers. All interface lines carry the same definition and timing conditions where commonality can be achieved. Some interface lines have different timing requirements because of the basic product characteristics. For specific product characteristics see Table 1; for additional product detail see SMD, MMD, FHT MMD, CMD, LMD, or FMD product specifications. The following Interface signals vary in the different products:

Tag 1	On Cylinder
Tag 2	Servo Clock
Index	Seek End
Sector	Servo Offset*
Seek Error	Write Protected
	Return to Zero

4.0 ACCESSORIES

Accessory items required, but not furnished with the device, are shown in Tables 2 through 6, also see Figure 1.

*Illegal operation on FHT MMD.

TABLE 1. PRODUCT CHARACTERISTICS

MODEL TYPE	PRODUCT TYPE	NO. HEADS (LOGICAL)	TRANSFER RATE	BYTES/ TRACK	BYTES/ CYLINDER	BYTES/ SPINDLE	CYLINDER/ DEVICE	FIXED HEAD CAPACITY	FIXED MEDIA CAPACITY	REMOVABLE MEDIA
9760/62	SMD	5 DATA 1 SERVO	9.677 MHz	20 160	100 800	41 428 800/ 82 958 400	411/823	NONE	NONE	ALL
9764/66	SMD	19 DATA 1 SERVO	9.677 MHz	20 160	383 040	157 429 440/ 315 241 920	411/823	NONE	NONE	ALL
9730-12/ 9730-24	MMD	2/4 DATA 1 SERVO	9.677 MHz	20 160	40 320/ 80 640	12 902 400/ 25 804 800	320	NONE	ALL	NONE
9730-12F/ 9730-24F	MMD	2/4 DATA 48 FIXED 1 SERVO	9.677 MHz	20 160	40 320/ 80 640 + FIXED HDS	12 902 400/ 25 804 800 PLUS 48 FIXED HEADS	320 + 12 FIXED HD	967 680	ALL	NONE
9730-80	MMD	5 DATA 1 SERVO	9.677 MHz	20 160	100 800	82 958 400	823	NONE	ALL	NONE
9730-80F	MMD	5 DATA 1 SERVO 48 OR 96 FIXED	9.677 MHz	20 160	100 800 + FIXED HDS	82 958 400 PLUS 48 OR 96 FIXED HEADS	823 + △1 10/20 △2 FIXED HEADS	967 680/ 1 935 360	ALL	NONE
9730-160	MMD	10 DATA 1 SERVO	9.677 MHz	20 160	201 600	165 916 800	823	NONE	ALL	NONE
9730-160F	MMD	10 DATA 1 SERVO 48 OR 96 FIXED	9.677 MHz	20 160	201 600 + FIXED HDS	165 916 800 PLUS 48 OR 96 FIXED HEADS	823 △4 5/10 △5 FIXED HEADS	967 680/ 1 935 360	ALL	NONE
9733-2	MMD	128 DATA FIXED, 1 SERVO	9.677 MHz	20 160	80 640	2 580 000	32	2 580 000	ALL	NONE
9733-5	MMD	256 DATA FIXED, 1 SERVO	9.677 MHz	20 160	80 640	5 160 000	64	5 160 000	ALL	NONE
9448-32	CMD	2 DATA 2 SERVO	9.677 MHz	20 160	40 320	32 578 560	823	NONE	16 MB	16 MB
9448-64	CMD	4 DATA 2 SERVO	9.677 MHz	20 160	80 640	65 157 120	823	NONE	48 MB	16 MB
9448-96	CMD	6 DATA 2 SERVO	9.677 MHz	20 160	120 960	97 735 680	823	NONE	80 MB	16 MB
9775	FMD	40 DATA 1 SERVO 96 FIXED	9.677 MHz	20 160	806 400 + FIXED HDS	679 795 200 + 96 FIXED HDS	843 + △3 FIXED HDS	1 935 360	ALL	NONE
9445	LMD	4 DATA EMB SERVO	9.677 MHz	20 672	82 688	17 033 728	206	NONE	8 MB	8 MB

NOTES:

△1 0.96 MB FHT OPTION HAS 3 HEADS IN LAST CYLINDER.

△2 1.92 MB FHT OPTION HAS 1 HEAD IN LAST CYLINDER.

△3 1.93 MB FHT OPTION HAS 16 HEADS IN LAST CYLINDER.

△4 0.96 MB FHT OPTION HAS 8 HEADS IN LAST CYLINDER.

△5 1.92 MB FHT OPTION HAS 6 HEADS IN LAST CYLINDER.

△6 THE DATA CAPACITY SPECIFIED IS BASED ON THE NUMBER OF EIGHT BIT BYTES THAT ARE RECORDED ON A TRACK. THE UNSECTORED CAPACITY DOES NOT INCLUDE AN ALLOWANCE FOR TOLERANCE GAPS.

A590C

TABLE 2. CABLES AND TERMINATORS

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO.
"A" Cable (Controller to Device) Standard, Flat	1	4,5	775642XX
"A" Cable (Device to Device) Standard, Flat	2	4,5	775642XX
"A" Cable (Controller to Device) Jacketed, UL Approved	1	4,5	823855XX
"A" Cable (Device to Device) Jacketed, UL Approved	2	4,5	823855XX
"A" Cable (Controller to Device) Shielded	1	4,5	823724XX
"A" Cable (Device to Device) Shielded	2	4,5	823724XX
"B" Cable (Controller to Device) Standard, Flat	3	4,5	775643XX
"B" Cable (Controller to Device) Jacketed, UL Approved	3	4,5	823857XX
"B" Cable (Controller to Device) Shielded	3	4,5	823659XX
Terminator, Flat	1	4,5,6,	75841300 75886100
TB216 Field Exerciser	7		82338800

NOTES:

1. One per device in star, one per multi-spindle installation in daisy chain.
2. One less than total devices in the system.
3. One per device
4. Last two digits of the part number denote cable length. For cable length See Table 3.
5. On systems using Dual Channel operation, twice the number of cables and terminators are required. CMD Drives are single channel only.
6. Terminator 75886100 to be used on CMD.
7. Quanity as required for regional maintenance.

TABLE 3. I/O CABLE LENGTH AND TABS

	PART NO. TAB									
Cable Length In Feet	5	6	8	10	15	20	25	30	40	50
"A" Cable, Flat 775642XX "A" Cable Shielded 823724XX	00	01	02	03	04	05	06	07	08	09
"A" Cable, Jacketed 823855XX	NA	NA	NA	03	04	05	06	07	08	09
"B" Cable, Flat 775643XX "B" Cable Jacketed 823857XX "B" Cable Shielded 823659XX	00	01	02	03	04	05	06	07	08	09

TABLE 4. DISK PACKS (SMD,CMD,LMD)

		DISK PACK DESCRIPTION				
PRODUCT DISIGNATION	NOTE	9760	9762	9764/66	9448	9455
Data Packs	2	9876 P/N 70439501	9877 P/N 70438001	9883-91 P/N 70430514	1204 P/N 76204000	1208 76210000
CE Alignment Packs	1	876-51 P/N 70439001	877-51 P/N 70438700	883-51 P/N 70430003	1204-51 Required 76204400	Not

NOTES:

1. Quantity as required for regional maintenance.

2. At least one per spindle.

TABLE 5. MAINTENANCE EQUIPMENT

DESCRIPTION	NOTE	PART NO.
TB304-B Field Exerciser	1,2,3	77449301
TB304-C Field Exerciser	1,3	77449302
TB216-A Field Exerciser	1,2,4	82338800
Head Alignment Kit	1	77440500

NOTES:

1. Quantity as required for regional maintenance
2. Includes head alignment capability.
3. Operates SMD, MMD but not CMD.
4. Operates SMD, MMD, CMD, LMD, and FMD.

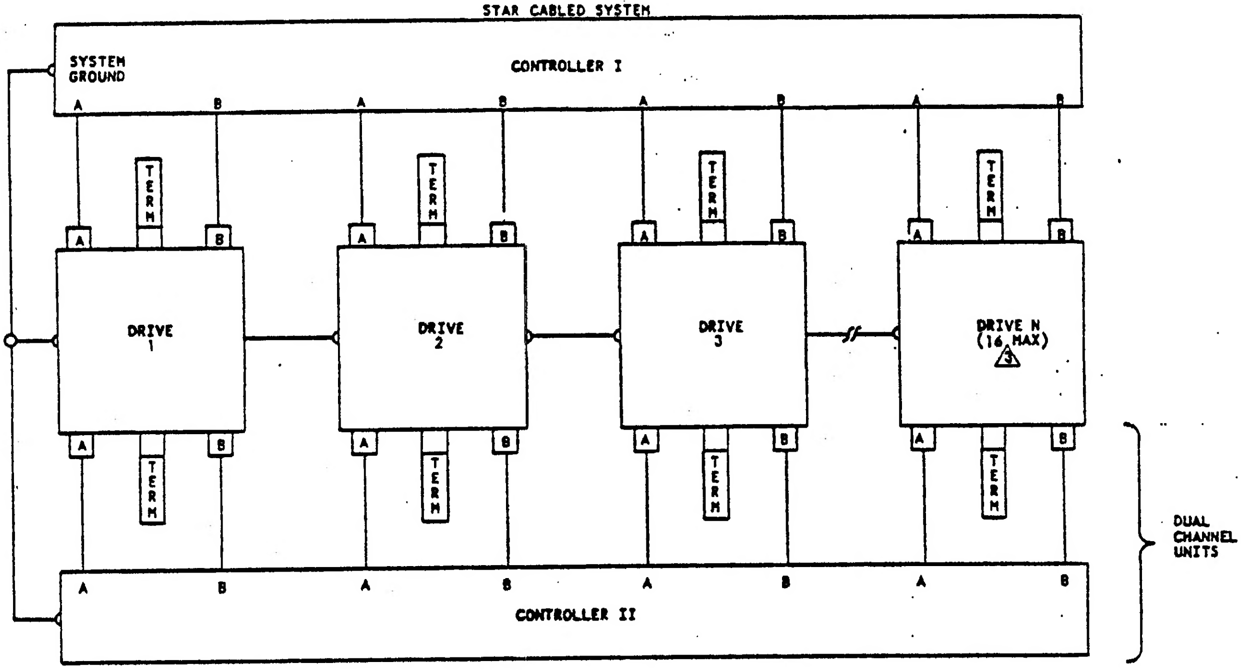
TABLE 6. MISCELLANEOUS HARDWARE

DESCRIPTION	QUANTITY REQUIRED	NOTE	PART NO.
Logic Plug	One per drive	1	943724XX
Single to Dual Channel (9764/66) Conversion Kit (9760/62)	One per drive		47205400 47205000
Single to Dual Channel (MMD) Conversion Kit (FMD)	One per drive		82348600 77842500

NOTE:

1. Last two digits denote lens tab, one set (0 through 15) is provided with each SMD and CMD. MMD and FMD logic number selection is done by switch in logic chassis. LMD Logic Number Selection is done by switch in power Input/Output (PIO) Module.

STAR CABLED SYSTEM



NOTES

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

△3 8 MAXIMUM FOR CMD CONFIGURATIONS.

DAISY CHAINED SYSTEM

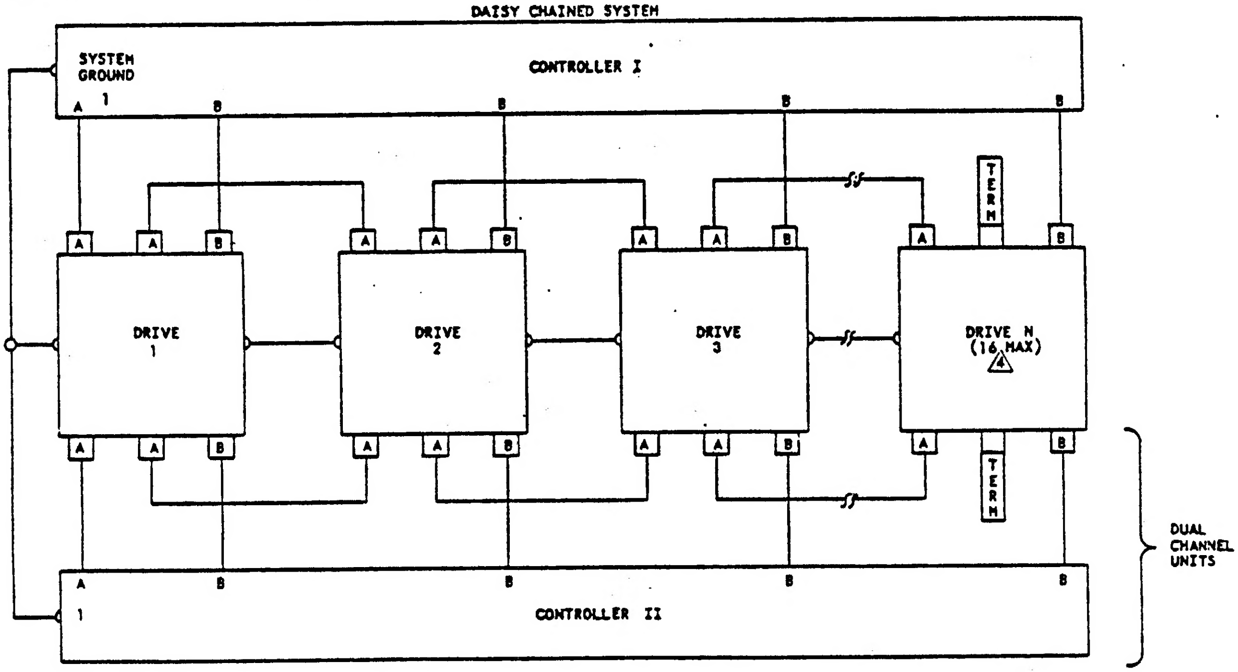


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FIGURE 1. UNIT CABLING

NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A STAR. SEE 6.1.4.1.
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER CARDS. SEE 6.1.4.2.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET.
MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET.
4. 8 MAXIMUM FOR CMD CONFIGURATION. 4 MAXIMUM FOR LMD CONFIGURATIONS

5.0 INTERFACE

5.1 Interface Definition

The standard "A" cable I/O is 60 pin configuration, the standard "B" cable is 26 pin configuration.

All input and output signals are digital, utilizing industry standard transmitters and receivers to provide a terminated, balanced, transmission system for long distances and/or noisy electrical environment.

The "A" cable is a twisted-pair, flat cable. The "B" cable is a ribbon flat-cable with ground plane and drain wire. Twisted pair and/or ground plane shielding is utilized to minimize crosstalk and reduce inductive coupling due to discharges, as well as control impedance variations regardless of cable lay.

5.1.1 Terminated, Balanced Transmission System

Transmitters and receivers of the industry standard types 75110A and 75108 or equivalent are used to provide a terminated, balanced transmission system (see Figure 2).

5.1.2 Line Transmitter Characteristics

The device controller line transmitters (see Figure 3) are compatible with the MPI line receiver described in 5.1.3.

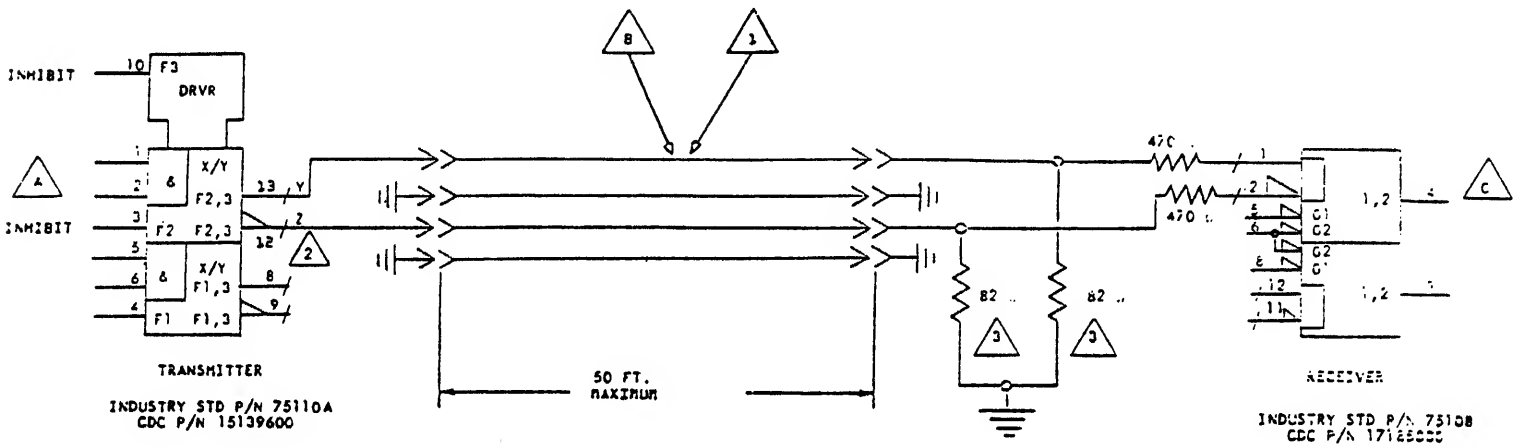
1. Output Signals Levels

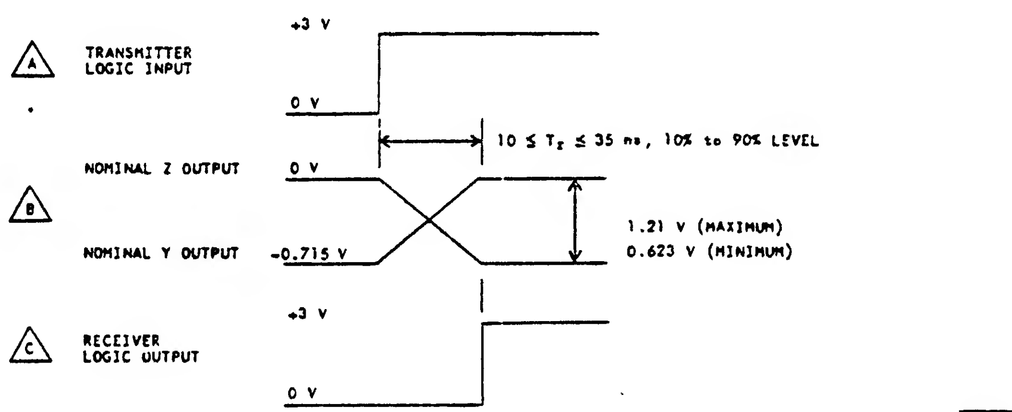
   Control Signals - See Figure 3
   Data Signals - See Figure 2

2. Output Line Polarity

   Control Signals - The MPI transmitter (see Figure 3) are connected to the I/O line such that the output, labeled Z, correspond with the low order pin number of the pin assignments and in turn connect to receiver pin labeled B, except for the Unit Selected line which is connected in the opposite manner.

   When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver, except for the Unit Selected line where a logical 1 into the transmitter produces a logical 0 out of the receiver.

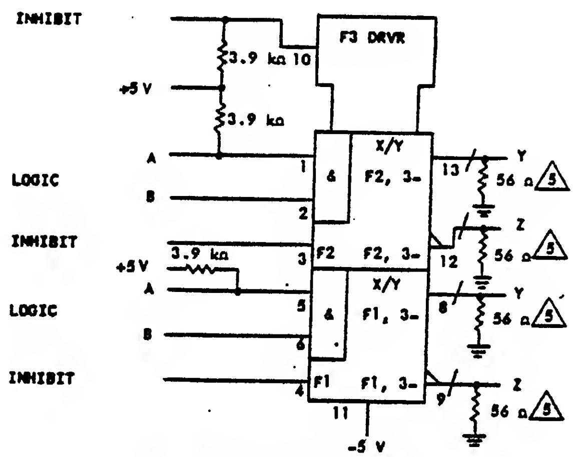




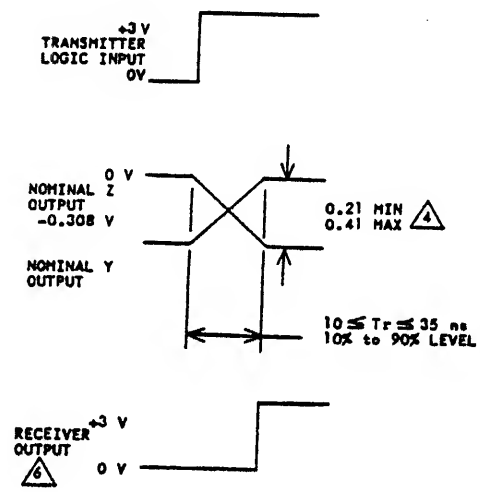
NOTES:

1. CABLE SHALL BE FLAT CABLE WITH CHARACTERISTIC IMPEDANCE 130 ±13 OHMS, CDC P/N 77564300 OR EQUIVALENT.
2. FOR LOGIC LEVELS AND TRUTH TABLE, SEE FIGURES 1, 2 AND 3.
3. TERMINATOR RESISTORS ARE LOCATED ON DRIVE LOGIC CARD OR IN CONTROLLER. THESE SIGNALS MUST BE STAR CABLED.

FIGURE 2. TYPICAL READ/WRITE DATA AND CLOCK TRANSMITTER AND RECEIVER



TRANSMITTER CDC P/N 15139600
(INDUSTRY STD P/N 75110A)



LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	F2	F1	Y	Z
L or H	L or H	L	L or H	H	△3
L or H	L or H	L or H	L	H	△3
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

TRUTH TABLE

S133A

NOTES:

1. OUTPUT LEVELS - L = MOST NEGATIVE LEVEL
   H = LEAST NEGATIVE LEVEL
2. INPUT LEVELS - H = MOST POSITIVE LEVEL
   L = LEAST POSITIVE LEVEL

△3 THIS IS AN INDETERMINATE INSTRUCTION WHEN SENSED BY AN ACTIVE (SELECTED) RECEIVER.

△4 VOLTAGE RANGE INCLUDES TRANSMITTER OUTPUT SWING IN LOW STATE OF 11 ±3 mA, AND A 5% TERMINATING RESISTOR OF 56 OHMS.

△5 TERMINATING RESISTORS ARE REQUIRED ON ALL "A" CABLE TRANSMITTERS. TRANSMITTERS IN THE DRIVE ARE TERMINATED BY THE TERMINATOR ASSEMBLY. REFER TO SINGLE AND DUAL CHANNEL INTERFACE ILLUSTRATION, AND THE TERMINATOR PARAGRAPH.

△6 RECEIVER INPUTS A AND B ARE CONNECTED TO TRANSMITTER OUTPUTS Y AND Z RESPECTIVELY.

FIGURE 3. CONTROL LINE TRANSMITTER

5.1.3 Input Amplifier (Receiver) Characteristics

The device controller input amplifier (see Figure 4) is compatible with the MPI transmitter described in 5.1.2.

1. Receiver Propagation Delay

   The receiver propagation delay is typically 17 ns in the direction of the logical 1, and 17 ns in the direction of the logical 0.

2. Receiver Input Polarity

   Control Signals - The input (labeled "B") of the receiver (see Figure 4) is connected to the lowest numbered pin of the pair in the cable and in turn connected to the transmitter pin labeled Z.

   Data Signals - See Figure 2.

5.1.4 Terminator

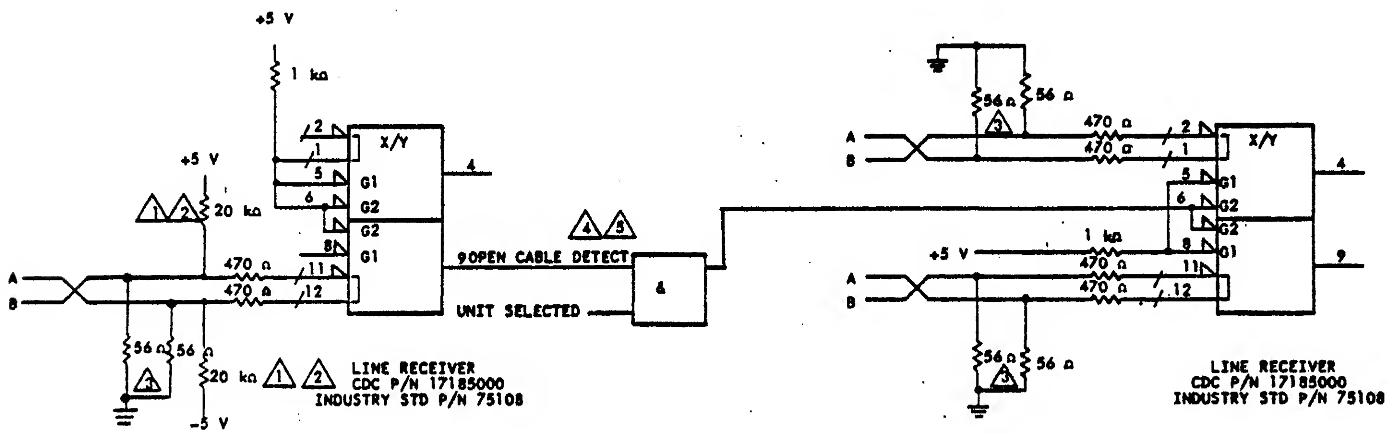
1. "A" Cable

   A terminator resistance as shown in Figures 3 and 4 is required at the transmitter and receiver end of each transmission line of the "A" cable. This resistance is provided on the unit by the terminator assembly which must be ordered separately.

   A termination resistance is required at the controller end of each line of the "A" cable except for the Open Cable Detect line (see 5.2.2(7)). No termination resistance is used on the Power Sequence lines in the "A" cable.

2. "B" Cable

   A termination resistance as shown in Figure 2 is required at the receiver end of each transmission line of the "B" cable. This resistance is provided at the unit's receiver logic card.



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DIFFERENTIAL INPUTS	INHIBIT		OUTPUT
	G1	G2	
$V_A - V_B \geq 25$ mV	L or H	L or H	H
$\lvert V_A - V_B \rvert < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	IND.
$V_B - V_A \geq 25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

LINE RECEIVER TRUTH TABLE

NOTES:

1. 20 kΩ RESISTORS ARE TYPICAL VALUES.
2. A BIAS NETWORK SHOULD BE USED TO PREVENT FALSE STATUS OR INTERRUPT CONDITIONS WHEN DRIVE POWER IS OFF AT CONTROLLER END OF UNIT SELECTED AND SEEK END SIGNALS.
3. TERMINATING RESISTORS ARE LOCATED:
   A. ON LOGIC CARD FOR "B" CABLE LINES.
   B. IN SEPARATE TERMINATOR ASSEMBLY FOR "A" CABLE.
4. SEE 5.2.2.7 FOR DESCRIPTION OF OPEN CABLE DETECT SIGNAL.
5. IF AN OPEN CABLE CONDITION IS DETECTED.

FIGURE 4. CONTROL LINE RECEIVER

5.1.5 I/O Cable Parts Description

Jacketed cables 823855XX and 823857XX available only as a UL approved assembly.

5.1.5.1 "A" Cable (Nonshielded)

DESCRIPTION	MPI P/N	BERG P/N	SPECTRA-STRIP P/N
Connector (60 pos)	94361115	65043-007	
Contact, insert	94245603	75691-007	---------
Flat cable (twisted-pair), 30 pair, 28 AWG	95043902	---------	455-313-060

5.1.5.2 "A" Cable (Shielded)

DESCRIPTION	MPI P/N	BERG P/N	BRAND-REX P/N
Connector (60 pos)	94361115	65043-007	--------------
Contact, insert	94245603	75691-007	--------------
Cable, miniature 30 twisted pair	95050600	---------	T-8649

5.1.5.3 "A" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI P/N	AMP P/N
60 pin, right angle header	94369804	3-86479-4
60 pin, vertical header	94385129	3-87227-0

5.1.5.4 "B" Cable (Nonshielded)

DESCRIPTION	MPI P/N	3M P/N
Connector (26 pos)	65853402	3399-3000
Connector Pull Tab	92004801	3490-2
Flat Cable (26 pos) with ground plane and drain wire.	95028509	3476-26

5.1.5.5 "B" Cable (Shielded)

DESCRIPTION	MPI P/N	BERG P/N	BRAND-REX P/N
Connector (26 pos)	94361105	65043-024	--------------
Contact, insert	94245603	75691-007	--------------
Cable, shielded 20 pair	94391800	---------	T-8277A

5.1.5.6 "B" Cable Mating Receptacle on Unit or Controller

DESCRIPTION	MPI P/N	AMP P/N
26 pin, right angle header	94369802	1-86479-0
26 pin, vertical header	94385106	1-87227-3

5.1.6 I/O Cable Characteristics

5.1.6.1 "A" Cable (Nonshielded)

Type: 30 twisted pair, flat-cable
Twists per inch: 2
Impedance: 100 ±10 ohms
Wire size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft
Maximum cable length: 100 ft cumulative
Voltage rating: 300 V rms

5.1.6.2 "A" Cable (Shielded)

Type: twisted pair
Twists per inch: 1.25
Impedance: 95 ohms ±10%
Wire size: 26 AWG, 7 strands
Diameter over conductor: 0.039 nominal
Diameter over insulator: 0.562 nominal
Propagation time: 1.6 to 1.8 ns/ft
Maximum cable length: 50 ft cumulative
Voltage rating: 300 V rms

5.1.6.3 "B" Cable (With Ground Plane)

Type: 26 conductor, flat cable with ground plane and drain wire
Impedance: 65 ohms (3M P/N 3476-26)
Wire size: No. 28 AWG, 7 strands
Propagation time: 1.5 to 1.8 ns/ft
Maximum cable length: 50 ft
Voltage rating: 300 V rms

5.1.6.4 "B" Cable (Non Shielded)

Type: Twinax
Impedance: 160 ±16 ohms
Wire size: 30 AWG, 7 strands
Diameter over outer insulator: 0.620 maximum
Propagation time: 1.5 to 1.8 ns/ft
Maximum cable length: 50 ft
Voltage rating: 300 V rms

5.2 Signal Lines

5.2.1 Address and Control Tag Functions (Received by the Unit)

Address and Control functions are transferred on 10 lines. The significance of the information on these lines is indicated by one of three tag lines (see Figures 5, 6A, B, and C; and 7).

5.2.1.1 Cylinder Address (Tag 1)

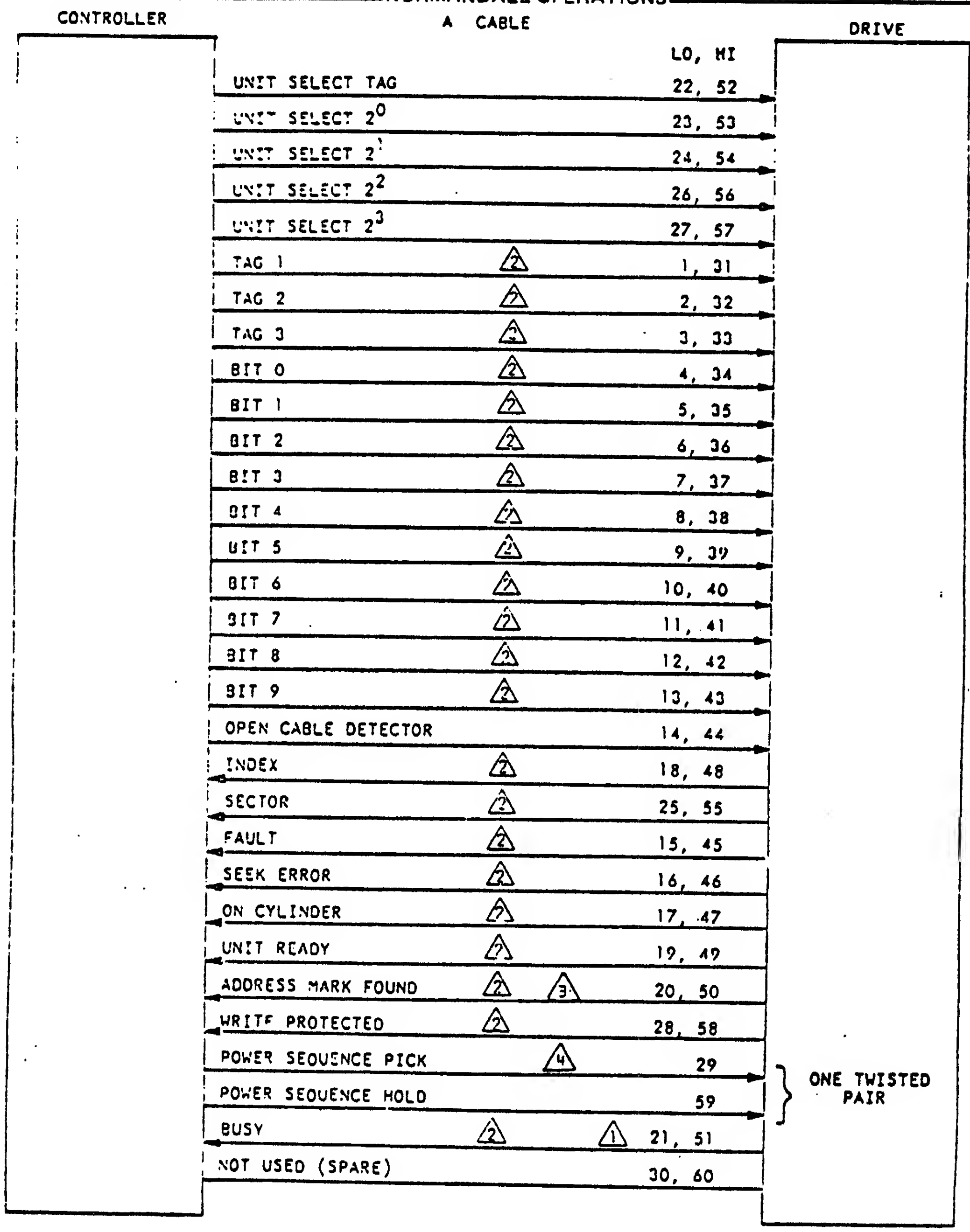
1. SMD, MMD, and FMD Moving Head

   Ten bus lines (Tag 1) are used to carry the Cylinder Address to the device. Since the device is a direct addressing device, the controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure 8A). The unit must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

2. CMD, LMD

   With the CMD, Tag 2 must precede Tag 1 when a volume change is made, that is, switching from fixed media to removable or removable to fixed. The correct servo head will be enabled at the trailing edge of Tag 1 (see Figure 8B).

   With the LMD, if the Seek-On-Head-change option is not selected, Tag 2 must precede Tag 1 when a head change is made (see Figure 8C).



I125E

NOTES: 60 POSITION
28 AWG, 30 TWISTED PAIR - STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT

1. DUAL CHANNEL UNITS ONLY.
2. GATED BY UNIT SELECTED.
3. ALWAYS A LOGIC ZERO OUTPUT IF LMD IS SELECTED.
4. DAISY CHAINED BUT NOT INTERPRETED BY LMD.

FIGURE 5. TAG BUS I/O INTERFACE

BUS	TAG 1 IN	TAG 2 IN	TAG 3 IN	UNIT SELECT
	CYLINDER ADDRESS	HEAD SELECT	CONTROL SELECT	
Bit 0	2^0	2^0	Write Gate	
1	2^1	2^1	Read Gate	
2	2^2	2^2	Servo Offset Plus 2	
3	2^3	2^3	Servo Offset Minus 2	
4	2^4	2^4	Fault Clear	
5	2^5		AM Enable	
6	2^6		RTZ	
7	2^7		Data Strobe Early	
8	2^8		Data Strobe Late	
9	2^9		Release 1	Priority Select 1

NOTES:

1 Dual Channel Only

2 Not used in FHT MMD

FIGURE 6A. TAG BUS DECODE SMD/MMD/FHT MMD

BUS	TAG 1	TAG 2	TAG 3
	CYLINDER ADDRESS	HEAD/VOLUME SELECT	CONTROL SELECT
BIT 0	2^0	2^0	Write Gate
1	2^1	2^1	Read Gate
2	2^2	2^2	Servo Offset Plus
3	2^3		Servo Offset Minus
4	2^4	2^4 △1	Fault Clear
5	2^5		AM Enable
6	2^6		RTZ
7	2^7		Data Strobe Early
8	2^8		Data Strobe Late
9	2^9		

NOTE:

△1 This bit is Volume Address which is stored in a bistable within the 9448 drive. The stored Volume Address and Tag 1 result in a Volume Select if the Cylinder Address is valid. (See flow chart for timing.) A zero denotes the removable cartridge and a one denotes the fixed disks.

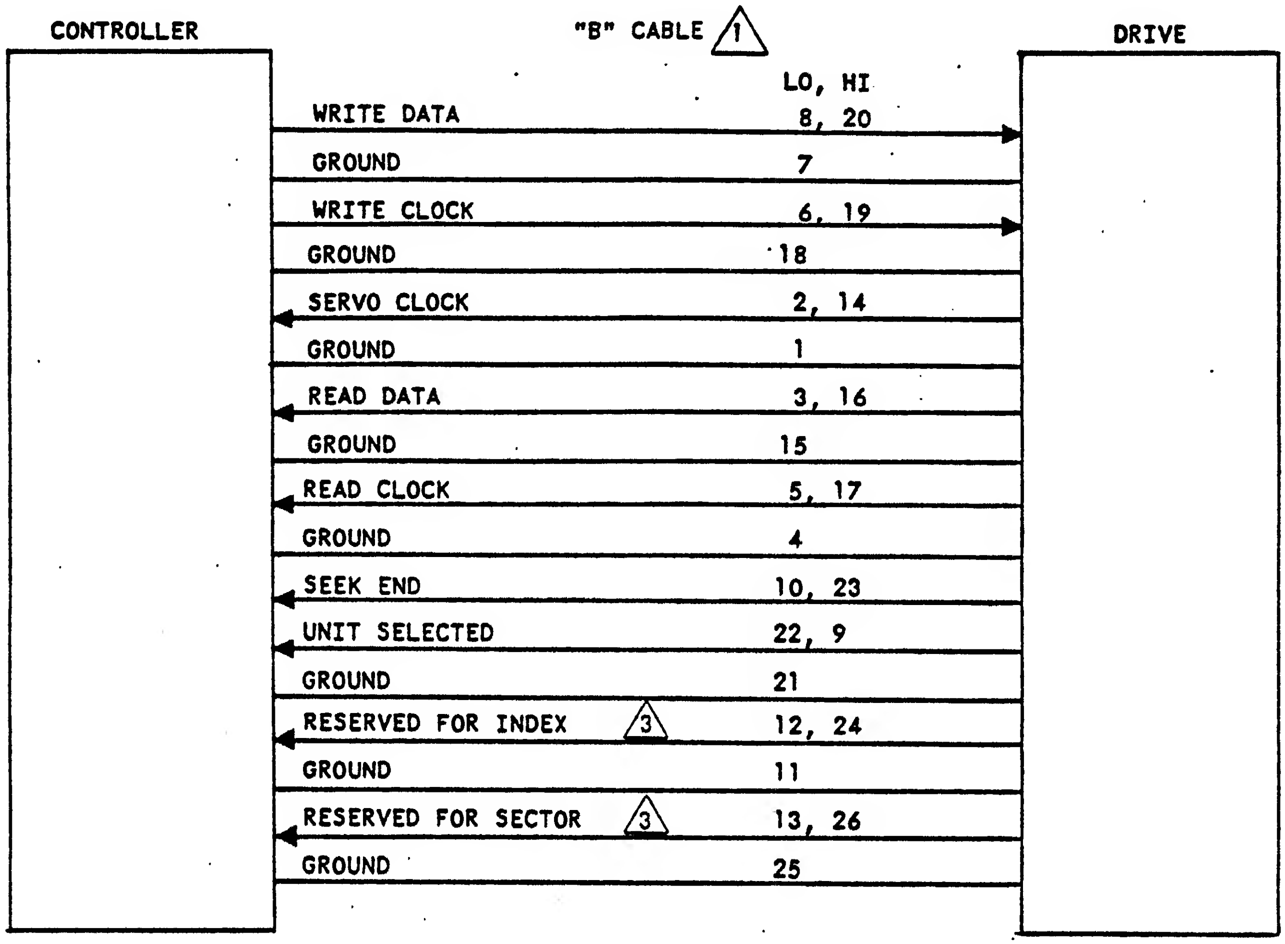
FIGURE 6B. TAG BUS DECODE - CMD

BUS	TAG 1 CYLINDER ADDRESS	TAG 2 HEAD/VOLUME SELECT	TAG 3 CONTROL SELECT
BIT 0	2^0	2^0 △1	Write Gate
1	2^1	2^1 △1	Read Gate
2	2^2	△2	Servo Offset Plus
3	2^3	△2	Servo Offset Minus
4	2^4	△2	Fault Clear
5	2^5	△2	△2
6	2^6	△2	RTZ
7	2^7	△2	Data Strobe Early
8	2^8	△2	Data Strobe Late
9	2^9	△2	△2

NOTES: △1 HEAD CHANGES ARE NOT INITIATED UNTIL A VALID SEEK IS RECEIVED FOLLOWING A HEAD CHANGE COMMAND IF THE SEEK-ON-HEAD-CHANGE OPTION IS NOT SELECTED. IF THE SEEK-ON-HEAD-CHANGE OPTION IS SELECTED, THE HEAD CHANGES AND A ZERO DISTANCE SEEK WILL BE INITIATED AS A RESULT OF THE HEAD CHANGE.

△2 NOT INTERPRETED BY THE LMD.

FIGURE 6C. TAG BUS DECODE-LMD



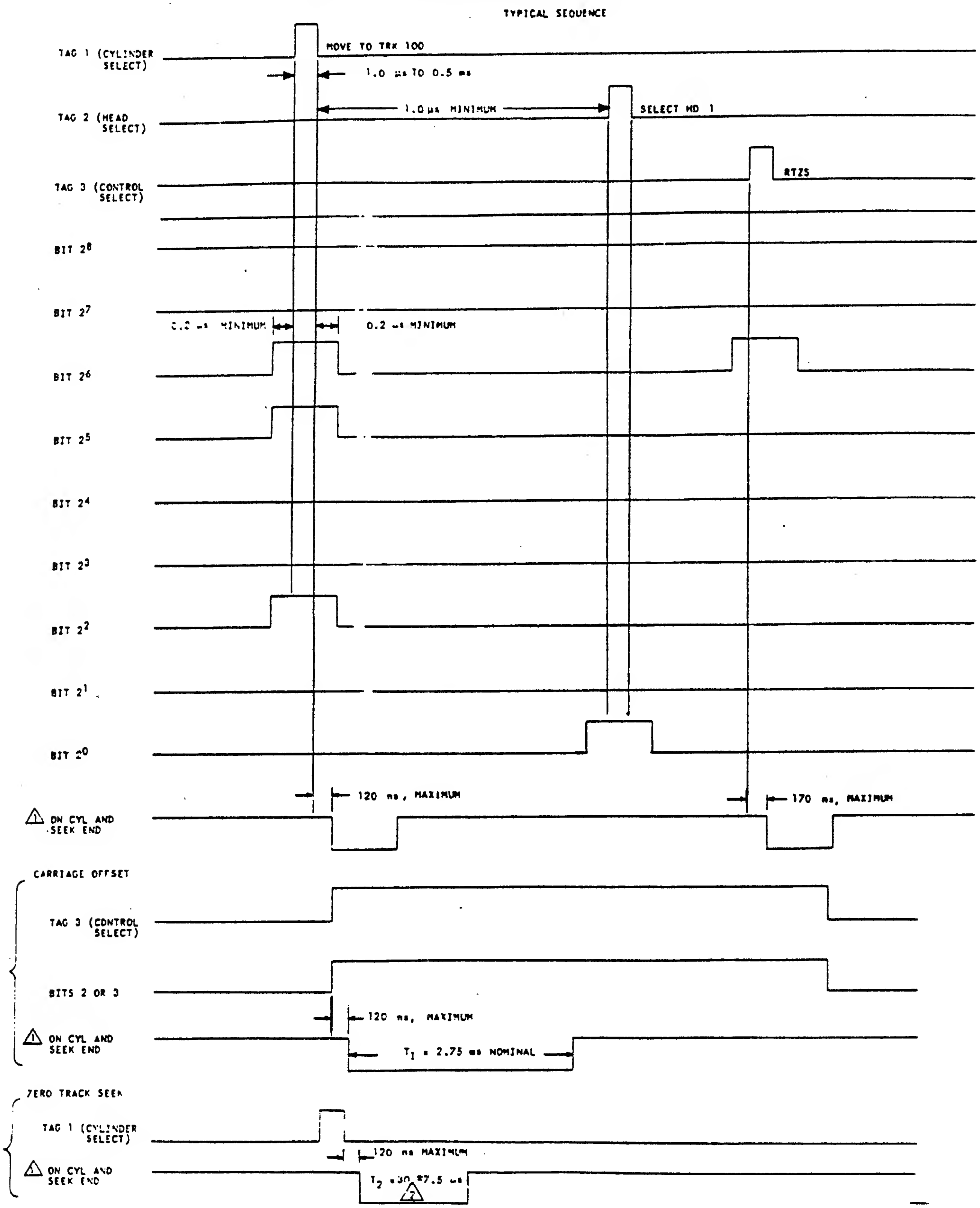
L46A

NOTES: 1 26 CONDUCTOR FLAT CABLE. MAXIMUM LENGTH - 50 FT.

2. NO SIGNALS GATED BY UNIT SELECTED.

3 THESE SIGNALS WILL BE PRESENT ON CMD AND LMD.

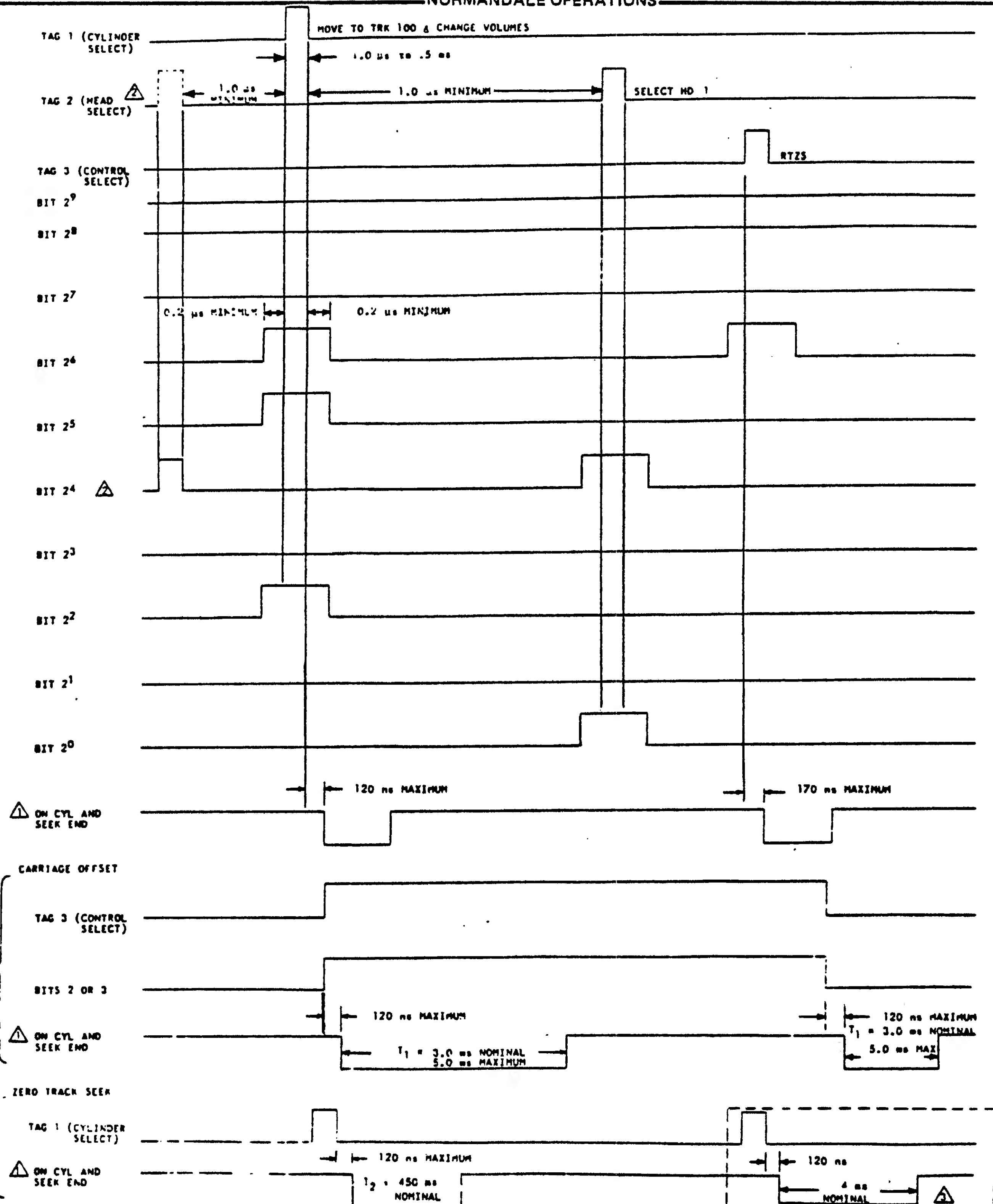
FIGURE 7. "B" CABLE INTERFACE



NOTES:

1. ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER, ALSO SEE 6.?.?.11.
2. T_2 . 150 ms MAXIMUM ... 80/160 MMD AND FMD.

FIGURE 8A. TAG AND BUS TIMING - SMD, MMD AND FMD (MOVABLE HEADS)



NOTES:
1. ON CYL AND SEEK END SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER, ALSO SEE 4.2.2.11.
2. TAG AND BUS TIMING REQUIREMENTS FOR A VOLUME CHANGE.
3. ZERO TRACK SEEK TIMING WITH VOLUME CHANGE.

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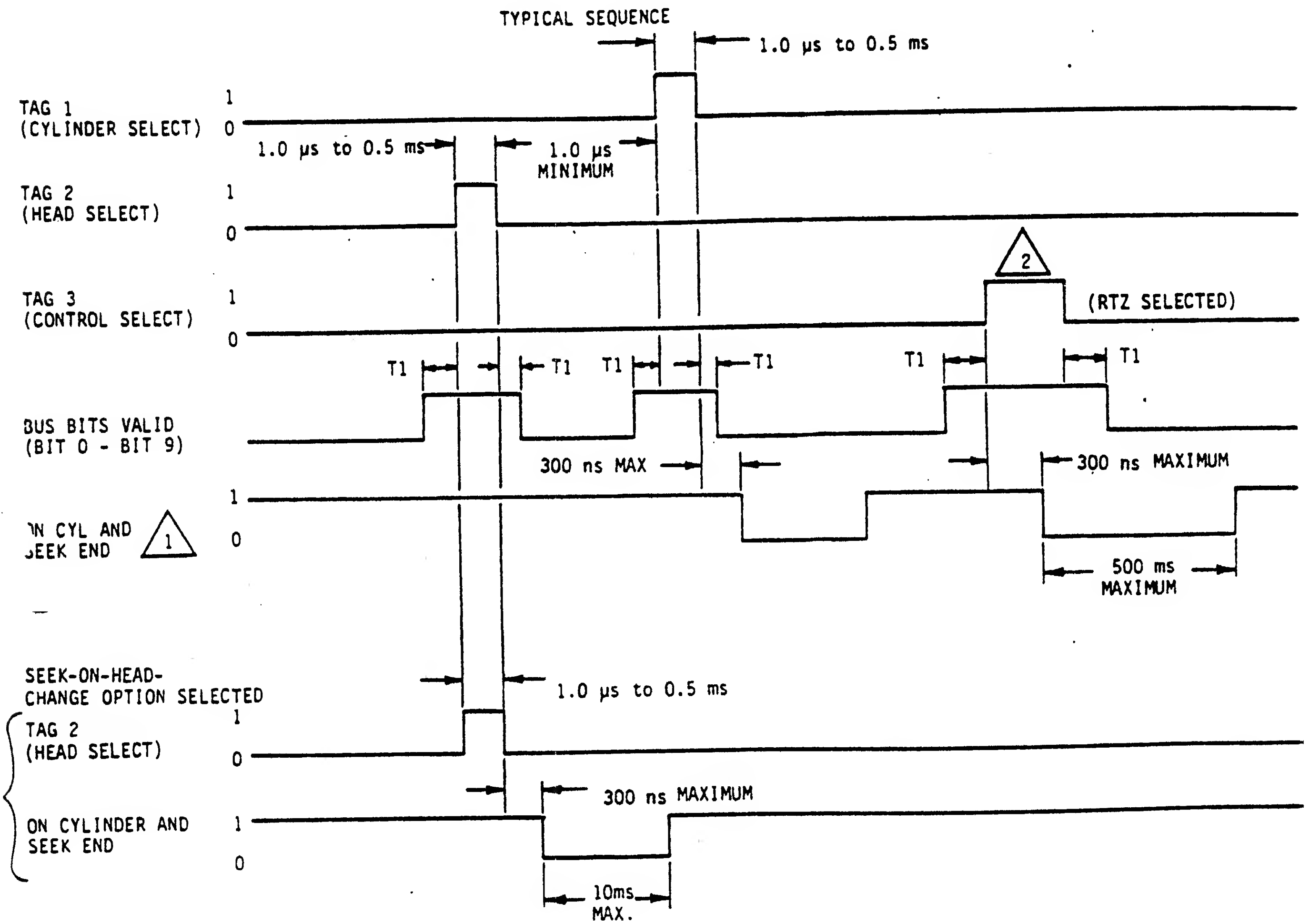
FIGURE 8B. TAG AND BUS TIMING - CMD



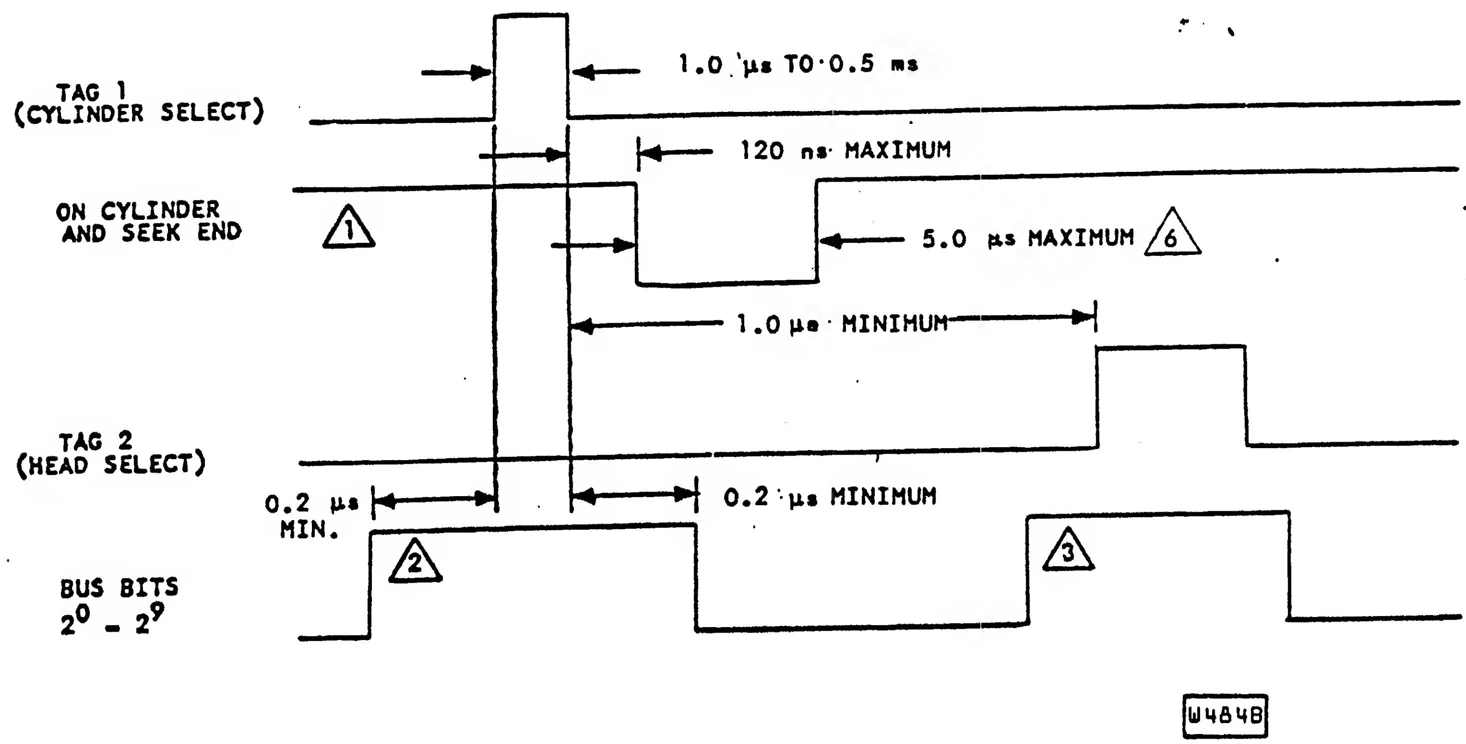
151A

NOTES: T1 = 200 ns MINIMUM

1. SEEK-ON-HEAD-CHANGE OPTION NOT SELECTED.

2. RTZ MAY ALSO BE GENERATED WITH TAG 3 STABLE (TRUE) AND BY STROBING THE APPROPRIATE BUS BIT.

FIGURE 8C. TAG AND BUS TIMING - LMD



NOTES:

1. TIMING SHOWN IS AT THE INPUT TO THE TRANSMITTER.
2. CYLINDER ADDRESSES 896-907 FOR FIXED HEAD (12 AND 24 MB).
   CYLINDER ADDRESSES 896/905/915 FOR FIXED HEAD (80 MB)
   CYLINDER ADDRESSES 896-898 FOR FIXED HEAD (680 MB).
   CYLINDER ADDRESSES 896/900/905 FOR 160 MB
3. HEAD ADDRESSES 0 TO 4 FOR FIXED HEAD.
   HEAD ADDRESSES 0 TO 39 FOR FIXED HEAD FMD (0 TO 15 ON CYLINDER 898).
4. TAG 1 AND TAG 2 MAY BE ISSUED IN EITHER ORDER PROVIDING 1.0 µs MINIMUM TIMING IS ALLOWED BETWEEN COMMANDS.
5. CYLINDER SELECT MUST BE REISSUED WHEN SWITCHING BETWEEN FIXED AND MOVABLE STORAGE.
6. 10 µs MAXIMUM FOR FHT MMD.

FIGURE 8D. TAG/BUS TIMING - FIXED HEAD MMD, FHT MMD

3. MMD and FMD Fixed Head Tag and Bus

Transfer of cylinder and head address information is controlled by the same timing requirements as the moving head sequence which is defined in Figure 8A. Because no positioner move is involved and it would be expected that a Head Select would immediately follow a Cylinder Select, the minimum Tag/Bus timing is as shown in Figure 8D.

The fixed heads may be used to either read or write data while the movable head positioner is in motion. The normal sequence of events would occur in the following order:

a. The controller issues a Cylinder Select with the desired movable head cylinder location on the bus. On Cylinder and Seek End will drop.

b. The controller accesses the desired fixed head location with the appropriate Cylinder Select and Head Select signals.

c. Conforming to the specified times for head select to read or write, the controller can read or write on the fixed head memory. The absence of On Cylinder and Seek End will not cause a fault in the unit when reading or writing on the fixed head shoe.

d. At the completion of the seek by the movable head positioner, On Cylinder and Seek End will become true.

e. When the Read or Write operation is complete on the fixed head, the controller may readdress the movable heads by sending the appropriate Cylinder Select (zero track seek) and Head Select signals. The Cylinder Select command is required in order to clear the Fixed Head mode.

4. FHT MMD Head and Tag Bus

Transfer of cylinder and head address information is controlled by the same timing requirements as the moving head sequence which is defined in Figure 8A. Because no positioner move is involved and it would be expected that a Head Select would immediately follow a Cylinder Select, the minimum Tag/Bus timing is as shown in Figure 8D. The normal sequence of events would occur in the following order:

a. The controller issues Cylinder Select Tag 1 (Cylinder Address Tag), and bus bits 0 through 31 for 2.5 MB (9733-2) or 0 through 63 for 5.0 MB (9733-5) units. On Cylinder and Seek End will drop.

b. The controller accesses the desired fixed Head Select with the appropriate head select signals. (See Head Select Tag 2 HPT MMD).

c. Conforming to the specified times for head select to read or write, the controller can read or write on the fixed head memory.

5.2.1.2 Head Select (Tag 2)

1. SMD

This signal is the Head Address that will be selectedby bits present on the bus lines when Tag 2 is true. The Logical/ Physical Addressing relationship for the SMD is in Table 7.

TABLE 7. LOGICAL/PHYSICAL ADDRESSING SMD

MEDIA DATA	SMD 40/80/MB	SMD 150/300 MB
Data surfaces/device	5	19
Movable heads/surface	1	1
Fixed heads/device	0	0
Movable cylinders/device	411/823	411/823
Fixed cylinders/device	0	0
Movable heads/logical cylinder	5	19
Fixed heads/logical cylinder	0	0
Movable cylinder addresses	0-410/0-822	0-410/0-822
Fixed cylinder addresses	-----	-----

2. MMD

This signal is the Head Address that will be selected by bits present as the bus lines when Tag 2 is true.

With the fixed head option incorporated in the MMD, the 48/96 physical fixed heads are addressed by the controller as logical cylinders. This addressing scheme allows maximum interface commonality with the moving head storage of the MMD and also with the SMD family. The logical/physical addressing relationship for these devices is summarized in Table 8.

TABLE 8. LOGICAL/PHYSICAL ADDRESSING MMD

MEDIA DATA	MMD 12 MB	MMD 24 MB	MMD 80 MB	MMD 160 MB
DATA SURFACES/DEVICE	1	2	5	5
MOVEABLE HEADS/SURFACE	2	2	2	2
FIXED HEADS/DEVICE	48	48	48/96	48/96
MOVEABLE CYLINDERS/DEVICE	320	320	823	823
FIXED CYLINDERS/DEVICE	12	12	10/20	5/10
MOVEABLE HEADS/LOGICAL CYLINDER	2	4	5	10
FIXED HEADS/LOGICAL CYLINDER	4	4	5 1 2	10 3 4
MOVEABLE CYLINDER ADDRESSES	0-319	0-319	0-822	0-822
FIXED CYLINDER ADDRESSES	896/907	896/907	896/905/915	896/900/905

NOTES:
1. 0.96 MB FIXED HEAD OPTION HAS 3 ADDRESSABLE HEADS IN CYLINDER 905.
2. 1.92 MB FIXED HEAD OPTION HAS 1 ADDRESSABLE HEADS IN CYLINDER 915.
3. 0.96 MB FIXED HEAD OPTION HAS 8 ADDRESSABLE HEADS IN CYLINDER 900.
4. 1.92 MB FIXED HEAD OPTION HAS 6 ADDRESSABLE HEADS IN CYLINDER 905.

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3. FHT MMD

This signal is the Head Address that will be selected by bits present on the bus lines when Tag 2 is true. The heads are addressed by the controller as logical heads and cylinders. This addressing scheme allows maximum interface commonality with the moving storage of the MMD and also with the SMD family. The logical/physical addressing relationship for these devices is summarized in Table 9.

TABLE 9. LOGICAL/PHYSICAL ADDRESSING FHT MMD

MEDIA DATA	FHT MMD 2.5 MB	FHT MMD 5.0 MB
Data surfaces/device	1	2
Fixed heads/device	128	256
Fixed cylinders/device	32	64
Fixed heads/logical cylinder	4	4
Fixed cylinder addresses	0 to 31	0 to 63

4. CMD

In the CMD this tag transmits Head and Volume Address bits on the bus lines to the device (see Figure 6B). This command must be followed by a valid seek command, (Tag 1) if the selected volume is different than the previously selected volume, since a volume change is not executed until the next valid cylinder address code (see Table 10). The Logical/Physical Addressing relationship for the CMD is summarized in Table 11.

TABLE 10. TAG 2. BUS DECODE FOR CMD

BUS BITS				HEAD SURFACE ID
2^4*	2^2	2^1	2^0	
0	0	0	0	HD No. 0 REM
1	0	0	1	HD No. 2 FXD
1	0	1	0	HD No. 3 FXD
1	0	0	0	HD No. 1 FXD
1	0	1	1	HD No. 4 FXD
1	1	0	0	HD No. 5 FXD

*This bit is Volume Address which is stored in a bistable within the 9448 drive. The stored Volume Address and Tag 1 result in a Volume Select if the cylinder address is valid.

TABLE 11. LOGICAL/PHYSICAL ADDRESSING CMD

MEDIA DATA	CMD 32 MB	CMD 64 MB	CMD 96 MB
Data surfaces/device	2	4	6
Movable heads/surface	1	1	1
Fixed heads/device	0	0	0
Movable cylinders/device	823	823	823
Fixed cylinders/device	0	0	0
Movable heads/logical cylinder	2	4	6
Fixed heads/logical cylinder	0	0	0
Movable cylinder addresses	0-822	0-822	0-822
Fixed cylinder addresses	-	-	-

5. LMD

In the LMD, this tag signifies that head and volume address bits are on the Bus lines to the device (See Figure 6C). This command must be followed by a valid seek command since a head change is not executed until the next valid cylinder address code is received via a Tag 1 function. Read or write commands will result in a Fault status until after the seek has been executed (see Table 12).

NOTE: Tag 2 must always be followed by Tag 1 (whether the head is different or the same).

On Cylinder will not become False as a result of a head change command alone.

Via a switch selectable Seek-On-Head-Change option within the LMD, a head select command will automatically initiate a head change and zero distance seek. "ON Cylinder" will go false for a maximum of 10 milliseconds. (See Figure 8C).

TABLE 12. TAG 2 BUS DECODE FOR LMD

BUS BITS		HEAD SURFACE IDENTIFICATION
2^1	2^0	Bus Bits
0	0	Top - Cartridge Disk
0	0	Bottom - Cartridge Disk
1	0	Top - Fixed Disk
1	1	Bottom - Fixed Disk

6. FMD

This signal is the head address that will be selected by bits present on the bus lines when Tag 2 is true.

With the fixed head option incorporated in the FMD, the 96 physical fixed heads are addressed by the controller as logical cylinders. This addressing scheme allows maximum interface commonality with the moving head storage of the FMD and also with the SMD and MMD family. The logical/physical addressing relationship for the FMD is summarized in Table 13.

TABLE 13. LOGICAL/PHYSICAL ADDRESSING FMD

MEDIA DATA	FMD 675 MB
Data surfaces/device	20
Movable heads/surface	2
Fixed heads/device	96
Moavable cylinders/device	843
Fixed cylinders/device	3
Movable heads/logical cylinder	40
Fixed heads/logical cylinder	40 1
Movable cylinder address	0-843
Fixed cylinder addresses	896-898

NOTE: 1 1.93 MB Fixed Head Option has 16 addressable heads in cylinder 898.

5.2.1.3 Control Select (Tag 3)

This signal acts as an enable and must be true for the entire control operation.

1. Write Gate (Bit 0)

   The Write Gate line enables the write driver (see Figure 6A, B, and C). See Figures 9A and B for typical Write Gate Timing requirements.

2. Read Gate (Bit 1)

   Enabling of the Read Gate (see Figures 6A, B and C) enables digital read data on the transmission lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern. (See Figures 9A and B for typical Read Gate timing.)

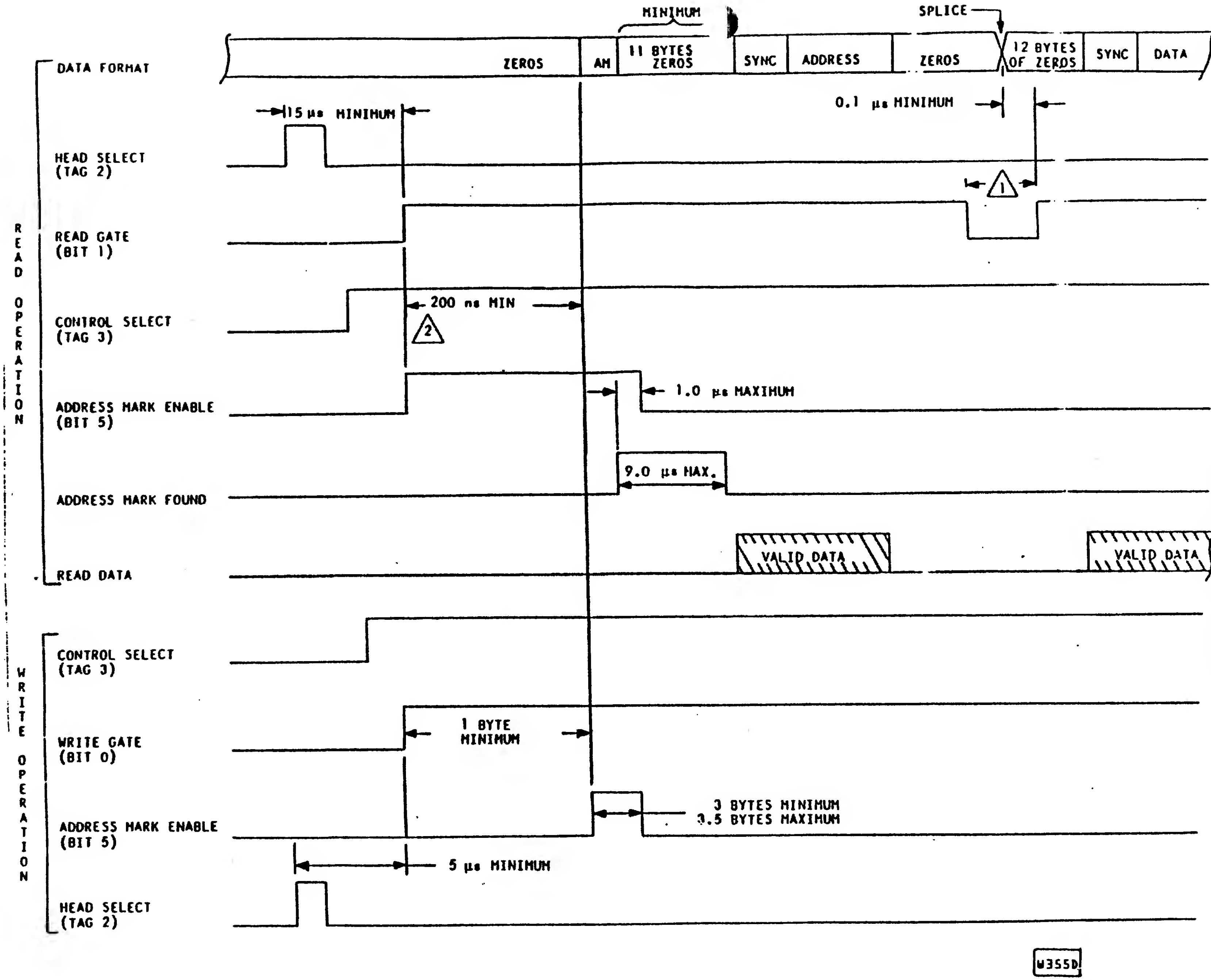
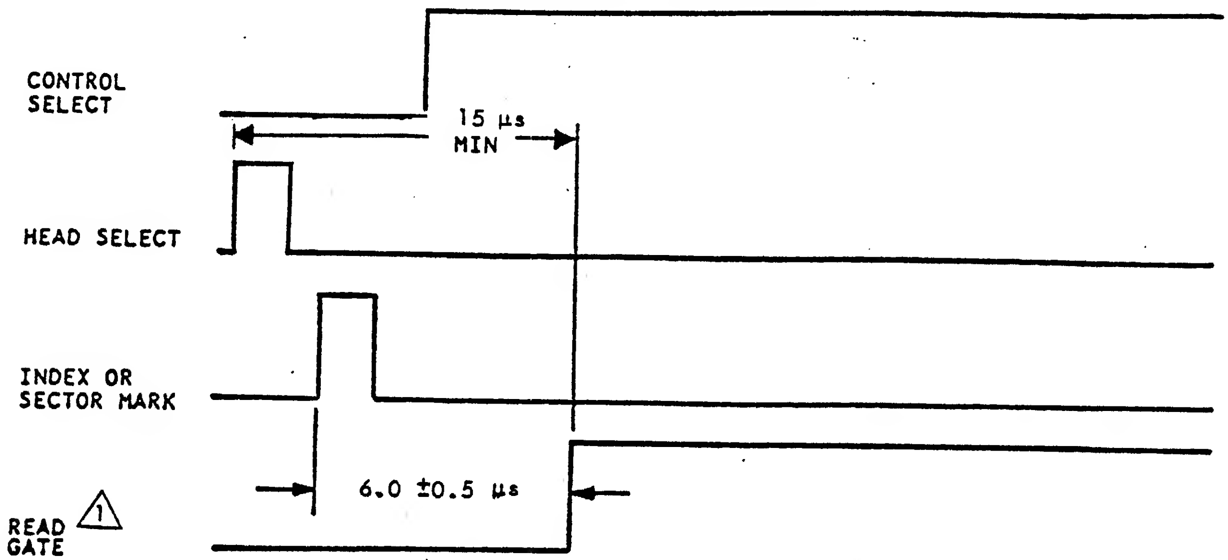


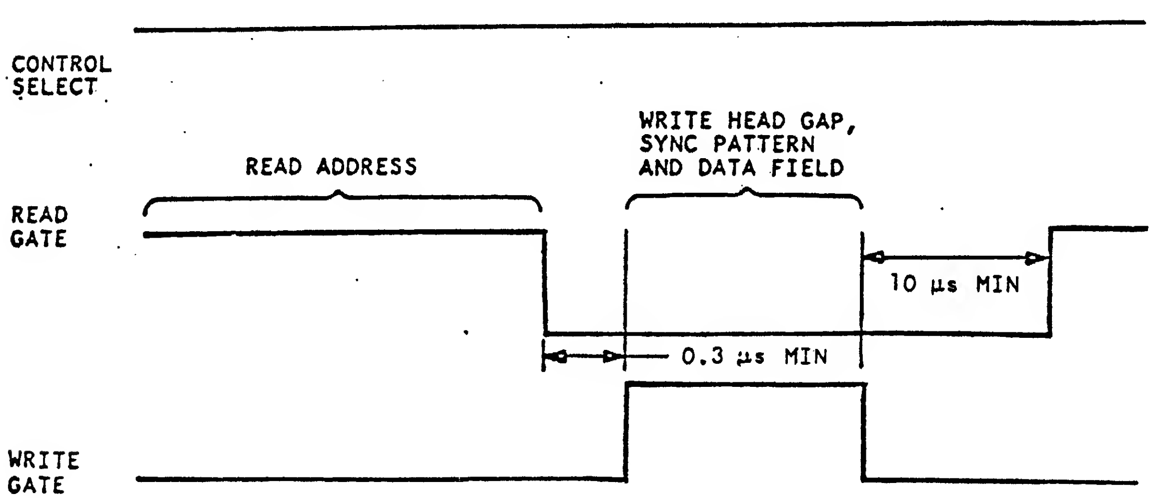
FIGURE 9A. CONTROL TIMING

NOTES: 1. READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 10 BYTES OF ZERO BITS REMAINING IN THE SYNC FIELD. 12 BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

2. ADDRESS MARK ENABLE SHOULD OCCUR SIMULTANEOUS WITH READ GA



A. TYPICAL READ CONTROL TIMING



B. TYPICAL WRITE CONTROL TIMING

W359D

NOTE: 1 IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR, READ GATE MUST NOT OCCUR LATER THAN 6.0 ±0.5 µs AFTER THE LEADING EDGE OF INDEX OR SECTOR.

FIGURE 9B. CONTROL TIMING

3. Servo Offset Plus (Bit 2)

SMD,CMD,FMD - When this signal is true, the actuator is offset from the nominal On Cylinder position towards the spindle. (See Figures 8A and B for timing.) When dropping Offset Plus, a 4 ms* delay is required before a read or write is initiated. When servo is in an Offset mode, no Write operation should be attempted.

MMD - When this signal is true, no physical movement of the heads is performed in the drive, used only to meet timing requirements of SMD drive family. (See Figure 8A for timing.)

FHT MMD - Same as MMD.

CMD only - If Write Gate is brought up when Offset is active, the Fault line will become true and Write Fault will set. A Fault Clear command must be issued to clear the fault condition.

LMD - This function is not executed by the LMD; however, On Cylinder will be deactivatd for 2 ms maximum from a logic change (i.e., 0 to 1 or 1 to 0) in this bit for flat cable interface compatibility.

4. Servo Offset Minus (Bit 3)

SMD/CMD/FMD - When this signal is true, the actuator is offset from the nominal On Cylinder position away from the spindle. (See Figure 8A and B for timing.) When dropping Offset Minus, a 4 ms* delay is required before a read or write is initiated. When servo is in an Offset mode, no write operation should be attempted.

MMD - When this signal is true, no physical movement of the heads is performed in the drive. Used only to meet timing requirements of SMD drive family. (See Figure 8A for timing.)

FHT MMD - Same as MMD.

CMD only - If Write Gate is brought up when Offset is active, the Fault line will become true and Write Fault will set. A Fault Clear command must be issued to clear the fault condition.

LMD - This function is not executed by the LMD; however, On Cylinder will be deactivated for 2 ms maximum from a logic change (i.e., 0 to 1 or 1 to 0) in this bit for Flat Cable Interface compatibility.

5. Fault Clear (Bit 4)

A pulse, 100 ns minimum, sent to the device will clear the Fault flip-flop if the fault condition no longer exists.

*CMD requires 5 ms without End Offset option.

LMD - A pulse, 300 ns minimum sent to the device will deactivate to logic 0 the fault condition within 2 ms measured from the leading edge of the Fault Clear pulse if the fault condition no longer exists.

6. AM Enable (Bit 5)

The AM (Address Mark) Enable line, in conjunction with Write Gate or Read Gate, allows the writing or recovering of Address Marks (see Figure 9A). When AM Enable is true while Write Gate is true, the writer stops toggling and erases the data, creating an Address Mark. Write Fault detection in the unit is inhibited during writing of an Address Mark.

When AM Enable is true while Read Gate is true, an analog voltage comparator detects the absence of Read signal. If the duration of the erased area is greater than 16 bits, an Address Mark Found signal will be issued.

NOTE: If Address Mark is not used, Bit 5 must be held to a logical 0 during control select functions.

LMD - Not interpreted

7. RTZ (Bit 6)

A pulse, 250 ns minimum, 1 ms maximum, sent to the device will cause the actuator to seek to track 0, reset the Head register, select the cartridge volume (CMD only), and clear the Seek Error flip-flop.

This seek is significantly longer than a normal seek to track 0, and should only be used for recalibration, not data acquisition.

This signal is used to select head zero, track zero, and clear Seek Error on the FHT MMD. Seek End and On Cylinder drop for 2.75 ms maximum.

LMD - A pulse, 300 ns minimum, 1 ms maximum, sent to the device will cause the actuator to seek track 0, select head zero, select the cartridge volume and deactivate to logic 0 the Seek Error status. The RTZ function will be completed in 500 ms maximum. On Cylinder will be false during the RTZ function. (Figure 8C).

8. Data Strobe Early (Bit 7)

When this line is true, the Device PLO Data Separator will strobe the data at a time earlier than nominal. Normal strobe timing will be returned when the line is false.

9. Data Strobe Late (Bit 8)

When this line is true, the Device PLO Separator will strobe the data at a time later than nominal. Normal strobe timing will be returned when the line is false.

NOTE: The Data Strobe signals are intended to be an aid in recovering marginal data. The data strobe position returns to nominal when the respective signals go false. The Data Strobe signals are only applicable while reading data from the disk.

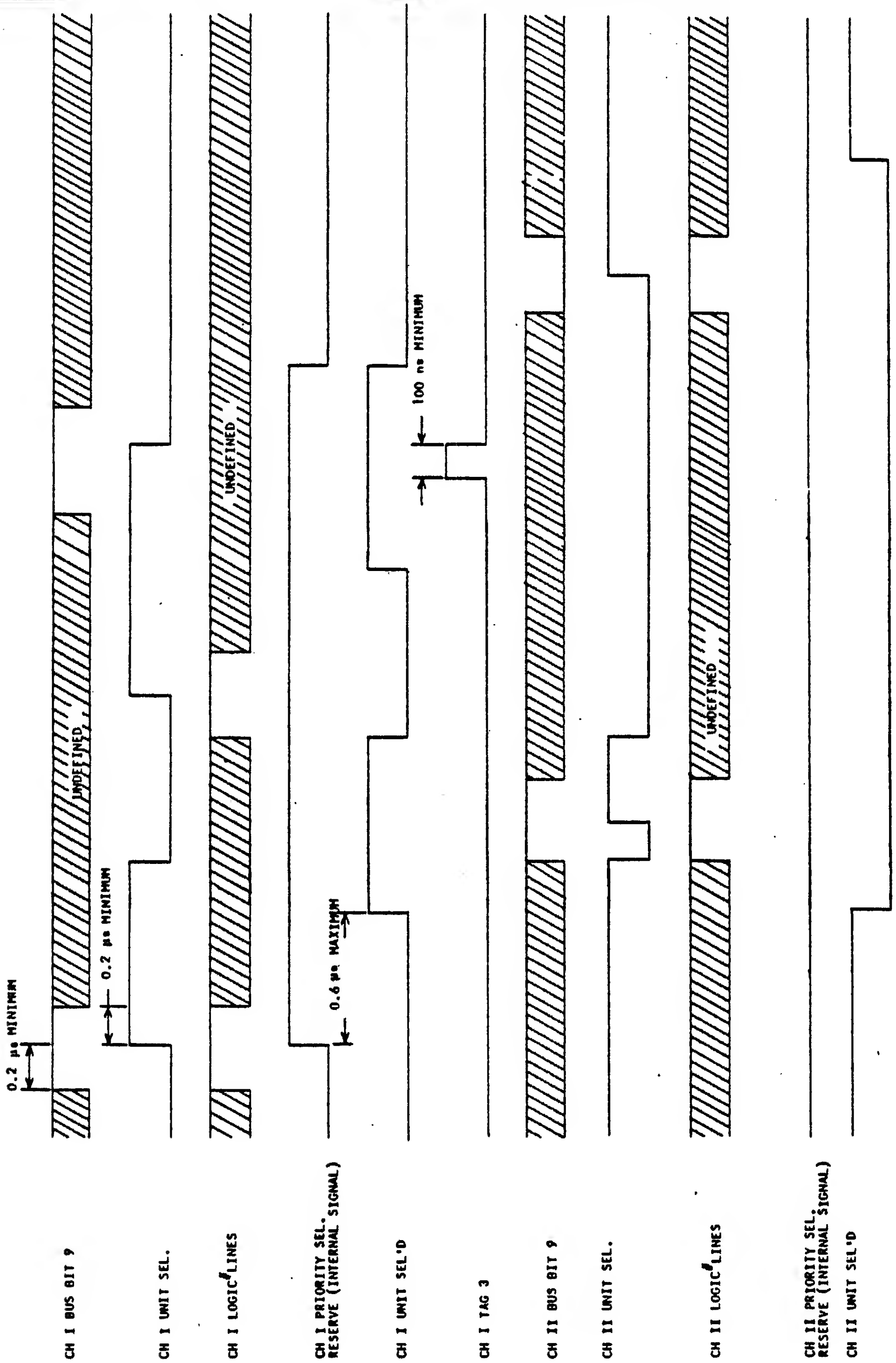
10. Release (Bit 9) (Dual Channel Only)

Enabling this line will release Channel Reserve and Channel Priority Select Reserve in the device, making alternate channel access possible after selection by the other channel ceases. If the unit is desired to function with Reserved Timer feature, Release will occur 500 ms nominal following the deselection of the device. If a longer or shorter time is desired, the timer may be customer altered by changing a resistor and capacitor to obtain delays from 500 ns to 10 seconds. Enabling Release will always clear Reserve and allow alternate channel access independent of the Reserve Timer feature. The Reserve Timer is enabled by means of a switch in the logic chassis. Inhibiting the Reserve Timer causes the device to stay reserved until specifically released by the operating channel. A unit is reserved immediately upon selection, but may be released any time after 500 ns following selection. By means of a switch in the logic chassis, it is also possible to absolutely reserve a device to one or other channels. For LMD, this signal is not interpreted.

5.2.1.4 Unit Select

Priority Select (Bit 9) (Dual Channel Only)

When this line is true, the unit will be unconditionally selected and absolutely reserved by the respective channel providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the Priority Select function has been performed the respective channel has exclusive access to the drive. The opposite channel can gain access only after a Release function has been performed on the selected channel (see 5.2.1.3-10). For timing see Figure 10. Following a Priority Select on one channel all interface signals are inhibited on the opposite channel including Unit Selected and Busy. For LMD, this signal is not interpreted.



SEQUENCE OF EVENTS

1. CH II SELECTED
2. CH I PRIORITY SELECT
3. CH II PRIORITY SELECT
4. CH I RELEASE
5. CH II SELECT

FIGURE 10. SAMPLE PRIORITY SELECT TIMING

5.2.2 Individual Lines

1. Sector Mark

a. SMD,MMD,FHT MMD,FMD

The Sector Mark is derived from the servo track. Timing integrity is maintained throughout seek operations (see Figure 11A). The number of sectors per revolution is switch selectable and is determined by counting Dibits/Sector Clocks. The switches are located on a card within the logic chassis. Each switch represents a fixed number of Dibits/Sector Clocks when closed.

Switch:	0	1	2	3	4	5	6	7	8	9	10	11
No. of dibits/ sector clock:	1	2	4	8	16	32	64	128	256	512	1024	2048

To calculate the proper switch positions for the number of sectors desired, use the following formula:

$$\frac{\text{Dibits or Sector Clocks/Revolution}}{\text{No. Sectors}} = \text{Dibits or Sector Clock Count/Sector}$$

Example for 8 Sectors: $\frac{13\ 440}{8} - 1 = 1679$ (-1 for SM Counter Reset)

close switch 10	=	1024
9	=	512
7	=	128
3	=	8
2	=	4
1	=	2
0	=	1
One Dibit or Sector Clock for SM Counter Reset	=	1
		1680 dibits or Sector Clock/Sector

Each dibit or Sector Clock (806 kHz Clock) is equivalent to 12 data bits.

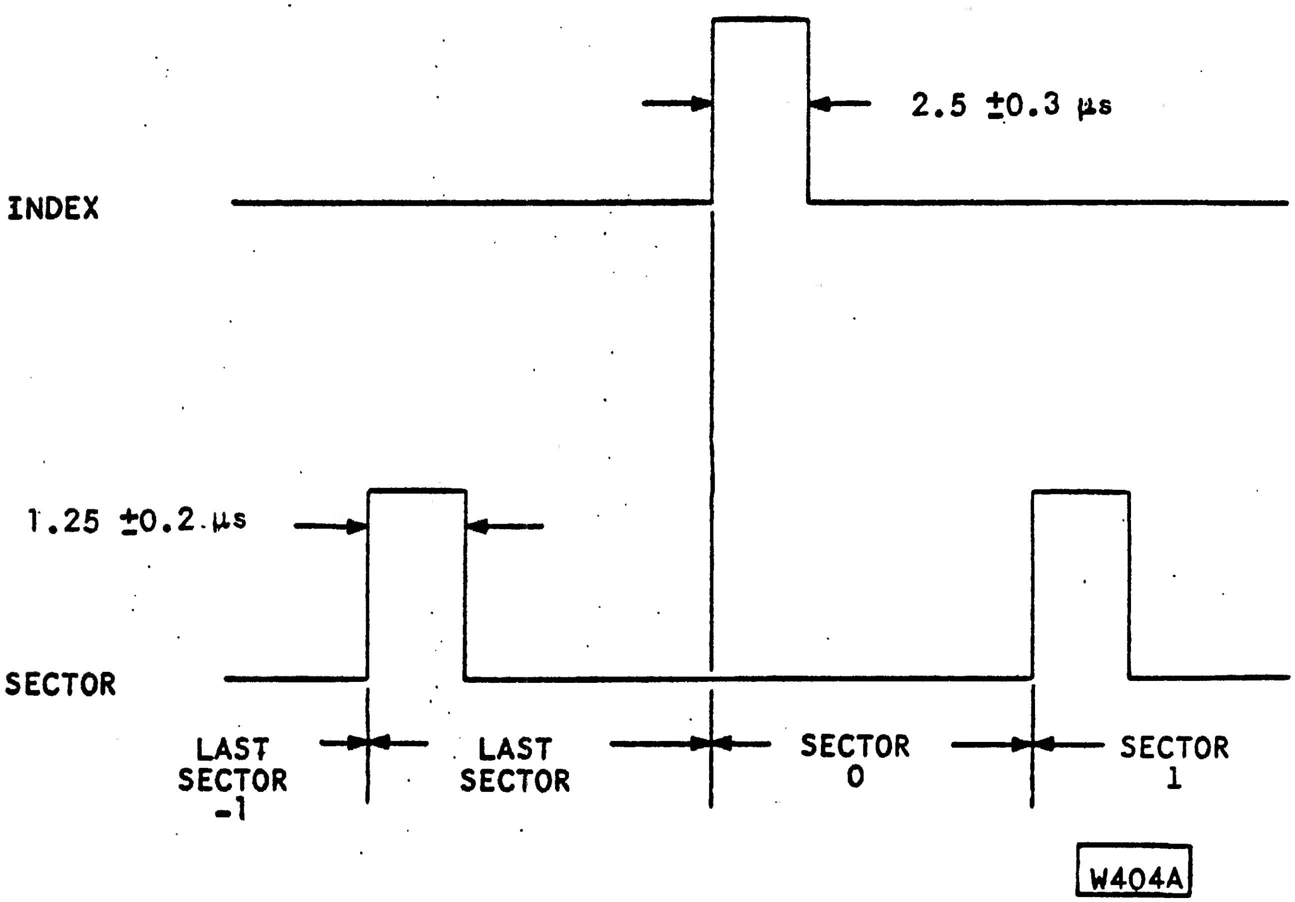


FIGURE 11A. INDEX AND SECTOR PULSES

b. CMD

The Sector pulse is derived from the servo track. Timing integrity is retained when Ready is active, and throughout seek operations in which no volume change is effected. There are 63 Sector pulses available per revolution (see Figure 11B). When combined with Index in the controller, this divides the tracks into 64 even length sectors. Other sector counts are available by changing the sector switches whose binary weight indicates the complement of the number of sectors desired. Sector pulses occur on both the A and B cables.

NOTES: The Sector pulses will be inhibited upon receiving the Cylinder Tag associated with a volume change until the detection of the first Index of the new volume (see Figure 11B).

Not all sector counts are even length. For example, a 50 Sector option would allow 50 even length sec- tors with an odd length sector at the end. The following even length sector counts are available: 4, 5, 6, 7, 8, 10, 12, 14, 15, 16, 20, 21, 24, 28, 30,32, 35, 40, 42, 48, 56, 60, 64, 70, 80, 84, 96, 105, 112, 120, and 128.

c. LMD

The Sector pulse (1.25 ±0.2 μs) is derived from the embedded servo information (see Figure 11C). Sector pulse integrity is maintained throughout all seek operations in which no head change is effected. There are 63 sector pulses available per revolution. When combined with Index in the controller, this divides the tracks into 64 equal length sectors. An alternate sector count of 32 equal length sectors is available via a different device configuration (i.e., a different assembly number).

NOTES: All sector pulses will be generated during a seek which requires no head change.

Some sector pulses will be omitted when a head change occurs (see Figure 11D). If the controller counts Sector pulses to determine sector location, the controller should wait until the next Index pulse following the completion of a seek with head change to determine the rotational position of the disk. Sector pulse timing integrity is not guaranteed while ON Cylinder is false during a seek after a head change.

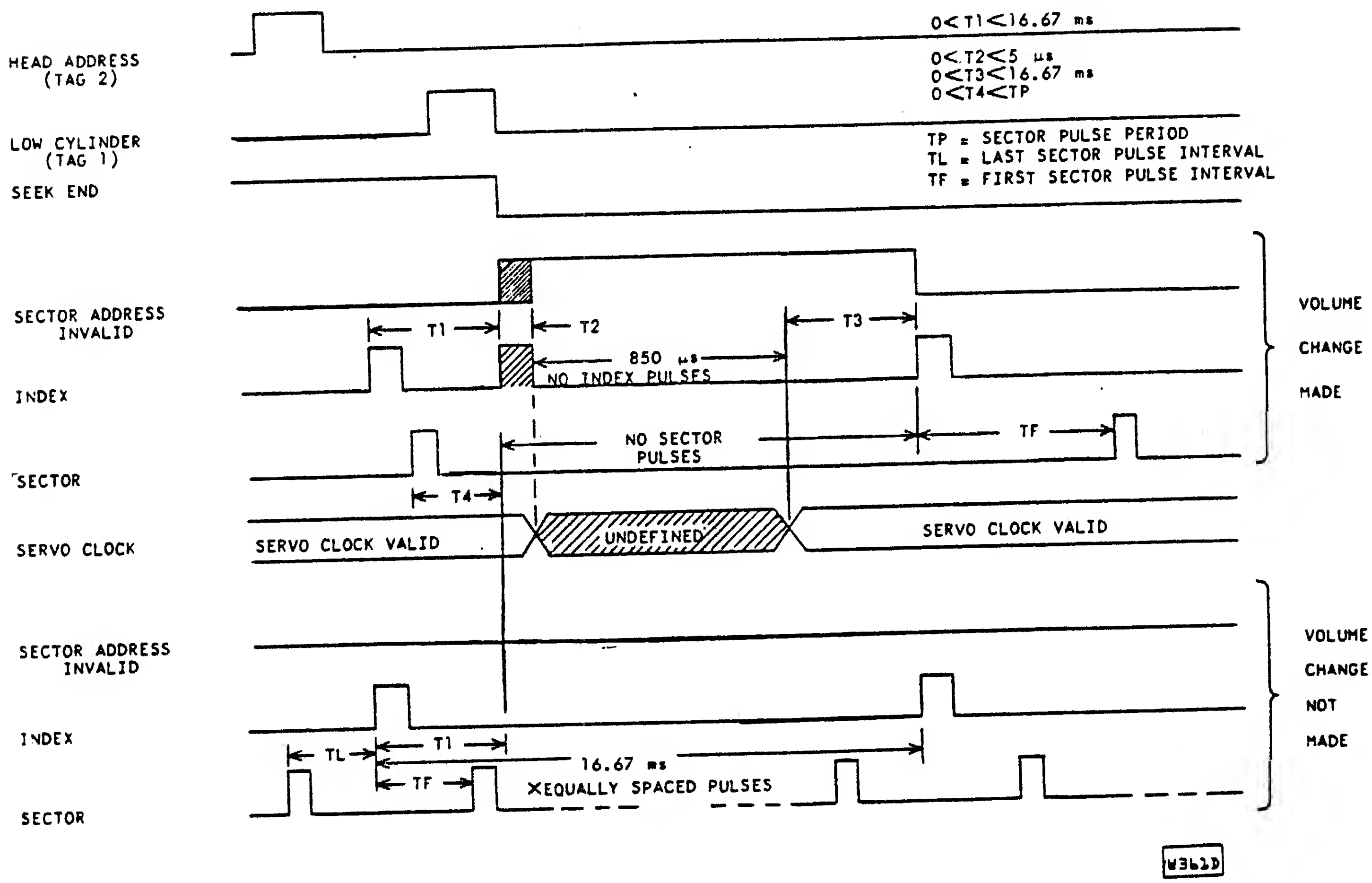


FIGURE 11B. INDEX AND SECTOR PULSES DURING SEEK - CMD

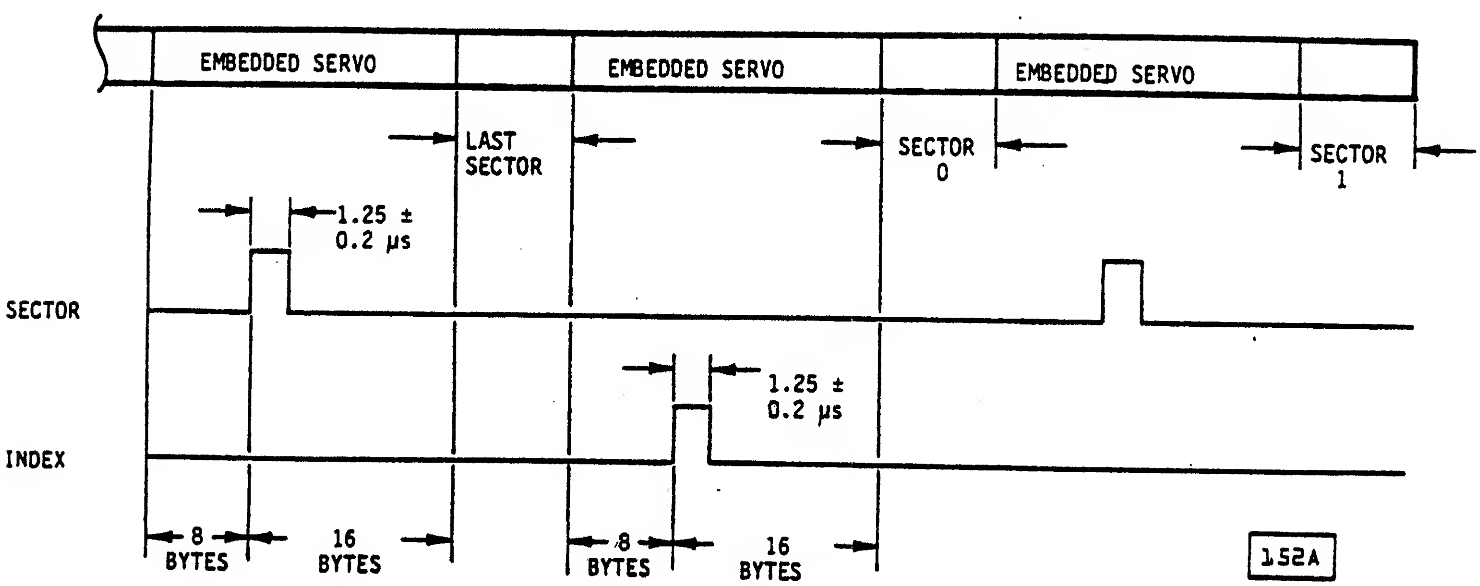
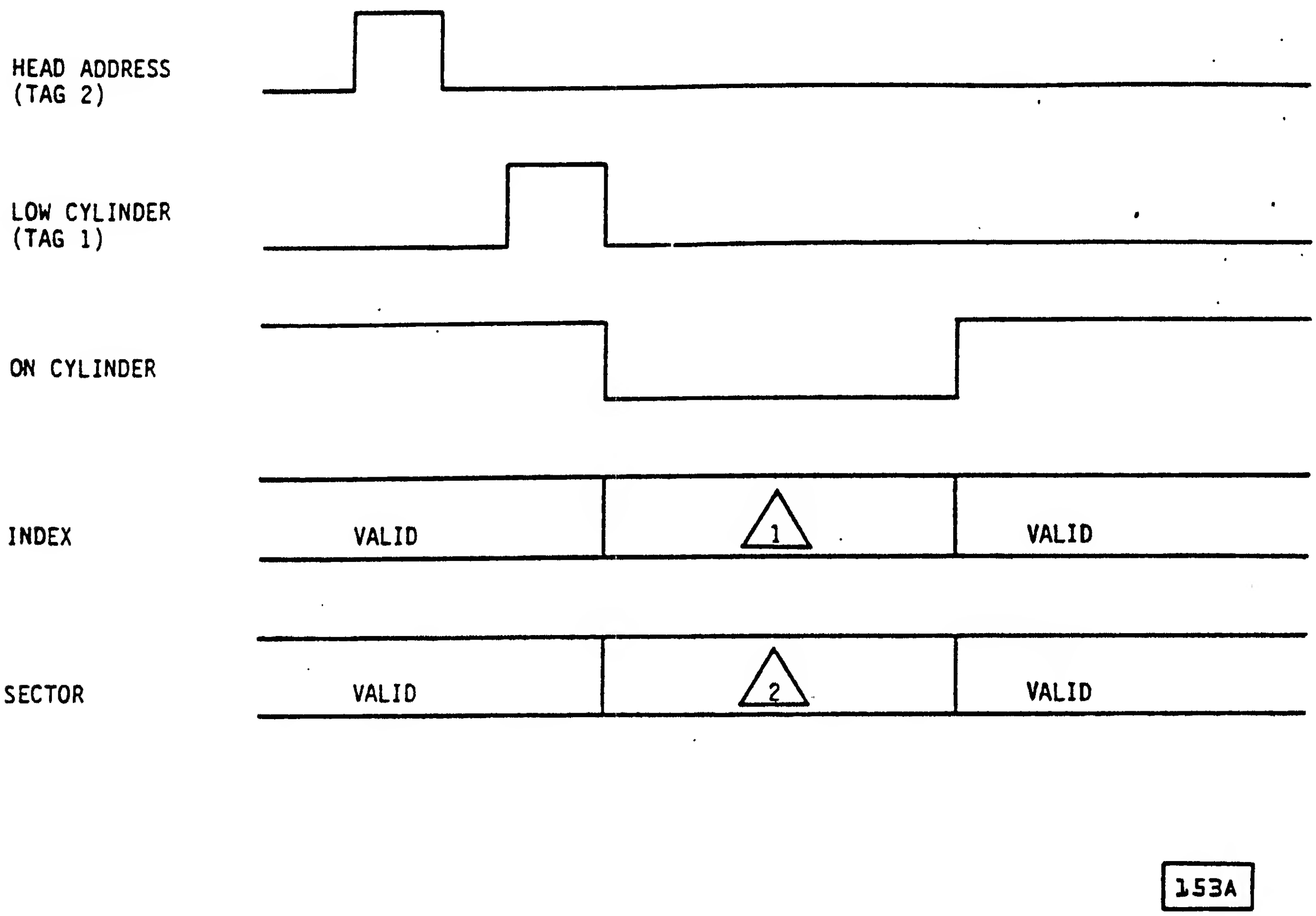


FIGURE 11C. INDEX AND SECTOR PULSES - LMD



1: DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN INDEX PULSES ARE POSSIBLE.

2: DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN SECTOR PULSES ARE POSSIBLE.

NOTE: 1) THE SERVO CLOCK TIMING INTEGRITY IS MAINTAINED DURING THE SEEK FUNCTION.

2) INDEX AND SECTOR TIMING INTEGRITY IS MAINTAINED IF NO HEAD CHANGE OCCURS

FIGURE 11D. INDEX AND SECTOR PULSES DURING SEEK - LMD

2. Fault

When this line is true, a fault condition exists in the device. The following types of faults may be detected by the device: DC Voltage fault, Head Select fault, Write fault, Write or Read while Off Cylinder, and Write Gate during a Read operation. A fault condition will immediately inhibit the writer to prevent data destruction. The DC Voltage fault indicates a below normal voltage from the positive or negative power supplies. The Head Select fault indicates that more than one head is selected. The Write fault indictes low (or the absence of) write current or the absence of write data.

This line may be cleared by Control Select, or Fault Clear on the operator panel, or Master Fault Clear on the Fault card (providing the fault no longer exists). Faults are also stored in individual flip flops as a maintenance aid, and may be cleared only by powering down dc power or clearing the fault by means of the switch on the fault card. The stored maintenance aid has no effect on unit operation.

LMD - This line will be deactivated within 2000 μs after activation of Fault Clear or by power sequencing the DC power to the unit (providing the fault no longer exists).

The fault conditions detected by the LMD may be grouped into the following four categories:

a. Interface Signal Related Faults

These types of faults indicated an attempted illegal operation by the interface controller. This type of fault may be generated by the detection of the interface Write Gate during a read operation, Write Gate or Read Gate while off cylinder, Write Gate and a write protected volume selected, Write or Read Gate after a head select and before a seek command, or Write Gate during the controller accessible section of a sector containing an unrecoverable embedded servo field.

NOTE: An LMD sector contains a drive interpreted embedded servo field followed by a controller accessible disk space for interface data storage/retrieval. The embedded servo field may not be read or written via the interface; however, a fault is not generated if the interface controller activates Read Gate or Write Gate during the embedded servo area. If the drive electronics is unable to properly recover an embedded servo area, any attempt to write in the succeeding sector area will generate a Write Fault.

b. Hardware Unsafe Faults Which Cause Head Retract

These types of faults indicate a detected drive hardware failure associated with the data read/write chain or the embedded servo internal protection electronics. These faults may be generated by a head failure i.e., open or shorted head, the loss of write current, the loss of Write Data during the Write Gate time, internal write enable during an embedded servo field, or absence of one of two required signals to the read/write electronics signifying the presence of an embedded servo field i.e., a redundancy check type feature.

c. Hardware Detected Faults Which Cause Head Retract

This type of fault, which indicates the loss of internal spindle motor speed control or improper servo positioning operation, will force a retract of the read/write heads. This type of fault may be created by the absence of embedded servo fields, an unsafe dc power voltage used by the head positioning electronics i.e., +5 V or ±16.5 V, or a below normal voltage on the emergency retract capacitor.

d. Microcomputer Detected Faults

A microcomputer within the LMD continuously monitors the drive performance to determine safe and reliable operation of the LMD servo and spindle motor electronics. A microcomputer detected fault may be created by the inability of the servo phase locked oscillator to maintain frequency synchronization for servo positioning control or data field write controk, out of tolerance spindle motor RPM, detection of the read/write heads positioned outside the valid data zones of the disk, or a failure of the drive to pass the power turn-on self test functions.

Certain microcomputer detected faults may lead to an emergency retract if the fault condition persists. Some faults indicate a Seek Error, and others indicate a need for maintenance though the LMD is still usable.

NOTE: CMD - For fault summary, see 7.2 in product SPEC 75888221.
FMD - For fault summary, see maintenance manuals 83323560,70

3. Seek Error

When this line is true, a Seek Error has occurred. The error may only be cleared by performing an RTZ. This signal indicates that the unit was unable to complete a move within 500 ms, (except MMD) or that the carriage has moved to a position outside the recording field or received an illegal track address. A Return-to-Zero Seek command will clear the Seek Error condition, return the heads to cylinder zero, and enable an On Cylinder signal to the controller.

SMD - If an address greater than 823 tracks (411 tracks for 9760/9764) is addressed, the Seek Error signal will go true within 100 ns of the Cylinder Select Tag, and the carriage movement is inhibited to one track or less.

MMD - 12 and 24 megabyte versions will not decode a Seek Error for an illegal track address until the positioner moves the heads into a guardband area. This requires approximately 65 ms under worst case conditions. There is no Seek Error status for cylinders beyond the designated fixed head cylinders.

The 80/60 megabyte version will decode a Seek Error for an illegal track address of 823 to 895 for the moving head portion. A Seek Error will also be decoded at cylinder 916 and above for fixed heads. The device will not decode a Seek Error in units without fixed heads or units with only one fixed head shoe (48 heads) if the designated fixed head cylinders are addressed. Response time for an invalid cylinder is 250 µs maximum.

MMD FHT - This signal indicates an illegal cylinder address.

CMD - If an address greater than 823 tracks is addressed, the Seek Error signal will go true within 450 µs maximum of the Cylinder Select Tag. Carriage movement is inhibited.

FMD - A Seek Error will be generated for an illegal track address of 844 to 895 and for tracks greater than 898. A Seek Error will be generated on track 898 if a head greater than 15 is selected.

LMD - If an address greater than 205 is attempted, the Seek Error signal will go true within 1.5 ms of the cylinder address Tag 1. Carriage movement is not attempted until a RTZ Command is received to deactivate the Seek Error signal.

4. On Cylinder

For all units except FHT MMD, this status indicates the servo has positioned the heads over a track. The status is cleared with any seek instruction causing carriage movements, or a zero-track seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms (nominal) for all devices.

SMD - For a zero track seek, On Cylinder drops for 30 μs nominal (see Figure 8A for timing).

MMD - For a zero track seek, On Cylinder drops for 30 μs nominal 12/24 MB, 150 μs maximum for 80/160 MB. For a seek to fixed head cylinders, On Cylinder drops for 5 μs maximum (see Figures 8A and D for timing).

FHT MMD - This signal indicates that a particular cylinder has been selected and the drive is ready to read or write.

CMD - For a zero track seek on the same volume, On Cylinder drops for 450 μs maximum. For a zero track seek with a volume change, On Cylinder drops for a 4 ms maximum (see Figure 8B for timing).

FMD - For a zero track seek, On Cylinder drops for 37.5 μs maximum. For a seek to a fixed head cylinder on cylinder drops for 37.5 μs maximum. (See Figure 8A and D for timing).

LMD - For a zero distance seek without a head change command, On Cylinder is deactivated for 1.5 ms maximum. For a zero distance seek with a head change, On Cylinder is deactivated for 10 ms maximum (see Figure 7D for timing). For logic changes i.e., either 0 to 1 or 1 to 0 in the Servo offset plus and minus commands, On Cylinder is deactivated within 300 ns and activated within 2 ms maximum for Flat Cable Interface compatibility.

5. Index

This signal occurs once per revolution, and its leading edge is considered the leading edge of the Sector Zero, typially 2.5 μs (see Figure 11A). Timing integrity is retained throughout seek operations for all devices.

CMD - Index will become invalid when a volume change is made. Index will remain invalid until the new servo head is selected and Index is properly decoded on the new volume. Index signal to the controller is gated off during a volume change. If volume switch occurs within an Index time, the pulse will not be gated off, it will be allowed its full time out. Upon changing volumes the first Index from the newly addressed volume may occur in an interval of from 650 µs to 20.5 ms after the volume change is initiated. Index occurs on both the "A" and "B" cables.

LMD - This signal occurs once per revolution and its leading edge is considered the sector pulse for sector zero; it is typically 1.25 µs (see Figure 11C). Index pulses may be missed when the seek command for a head change is performed. The index timing will become valid when On Cylinder becomes true following the seek function. (see Figure 11D). If a head switch occurs during an Index pulse, the pulse width is not affected.

6. Unit Ready

When true, and the device is selected, this line indicates that the device is up to speed. The heads are positioned over the recording tracks, and no fault condition exists within the device.

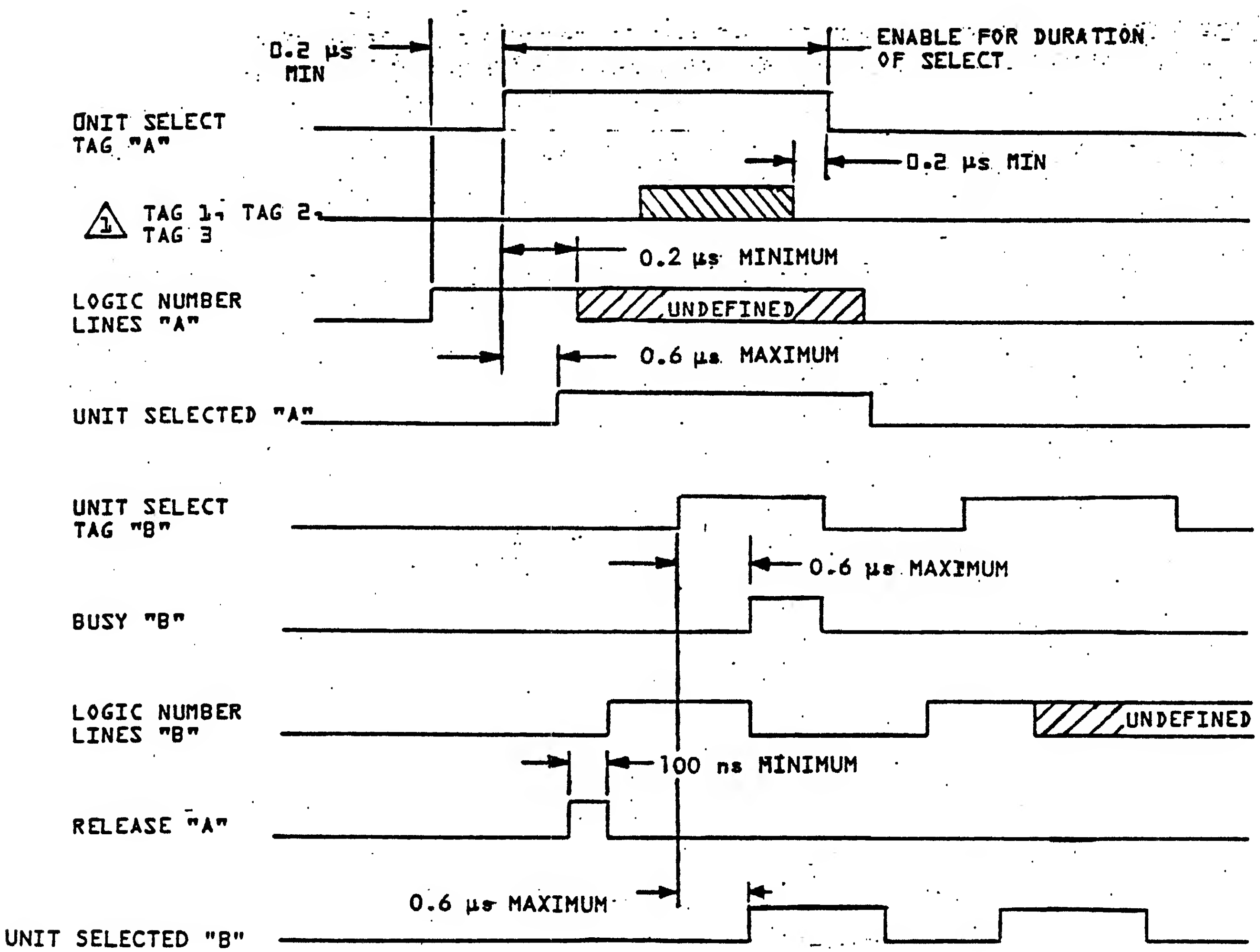
7. Open Cable Detector

The Open Cable Detect circuit (see Figure 4) disables the interface in the event that the "A" interface cable is disconnected or controller power is lost.

It is recommended that the controller circuitry have sufficient voltage margins and interlocks to prevent operation on the drive before the controller is Ready or prior to impending controller power failure. Relay logic and passive terminations sometimes aid this requirement. If 75110A transmitters are used to drive the Open Cable Detect line from the controller, two transmitters should be paralleled, and no 56 Ω termination resistance to ground should be used at the controller end.

8. Unit Select Tag

This signal gates the desired logic number into the Logic Number Compare circuit. The unit will be selected internally 600 ns maximum after leading edge of this signal. For timing see Figure 12. Note that this function must be edge triggered.



1 ALTHOUGH NOT FUNCTIONALLY INVOLVED IN THE UNIT SELECTION/DESELECTION OPERATION, TAGS 1,2, AND 3 MUST BE IN THE INACTIVE STATE AT LEAST 0.2 µs BEFORE DESELECTION TO INSURE I/O INTEGRITY.

1508

FIGURE 12. LOGIC NUMBER SELECT AND TIMING DIAGRAM

In Dual-Channel units, Unit Select Tag also forces the device to be reserved to that channel, providing selection occurs. The Reserve will not be cancelled unless by Release command, Reserve Timer or dc power-down/power up. If Bus Bit 9 and the desired logic number is present with Unit Select Tag, a Priority Select will be performed, see 5.2.1.4. The unit will be selected internally 600 ns maximum after leading edge of Unit Select Tag. For timing see Figure 12. If both controllers request access simultaneously, Channel "A" will be granted priority.

9. Unit Select (2^0, 2^1, 2^2 and 2^3)

These four lines are binary coded to select the logical number of 1 of 16 devices. The unit number (0 through 15) is selectable by means of switches located on a card in the logic chassis (MMD and FMD) or on a logic plug on the unit's operator panel (SMD).

NOTE: The CMD is limited to a maximum of 8 devices with logical addressing of (0 to 7) selectable by a logic plug on the operator panel.

LMD - These four lines are binary coded to select the logical number of 1 of 4 LMD devices. The unit number (0 through 15) is selectable by means of switches located on a card within the PIO. A maximum of 4 LMDs per system are allowed (see Figure 1).

10. Address Mark Found

Address Mark Found is a pulse which is sent to the controller following recognition of at least 16 missing transitions and the first zero of the zeros pattern.

The controller must drop the Address Mark Enable line (Bit 5) upon receiving Address Mark Found (AMF) and valid data will be presented on the I/O lines following the AMF pulse. Upon sensing the dropping of Address Mark Enable line, the Address Mark Found pulse will be reset within 8.0 μs maximum (see Figure 9).

NOTE: Under certain conditions it is possible that the MMD or FHT MMD could issue a false Address Mark Found signal during an address mark search operation. This would occur if a media flaw existed which simulated the electrical characteristics of an Address Mark (at least 16 missing transitions followed by a zero).

It is recommended provisions be made in system hardware or software to allow recovery from, or avoid the possibility of detecting false AMF signals.

LMD - This signal is not activated by the LMD but is daisy chained at the connector. This signal output will always be a logic zero.

11. Unit Selected

When the four Unit Select bit lines compare with the settings of the Unit Select switches in the logic chassis, and when the leading edge of Unit Select Tag is received, the Unit Selected line becomes true and is transmitted to the controller on the "B" cable (see Figure 11). Multiple Unit Selected responses on a daisy-chain system indicate duplicate switch settings have been used.

12. Write Protected

Enabling the Write Protect function inhibits the writer under all conditions, illuminates a LED located on logic cards in the MMD and FMD and on the operator panel in SMD, CMD and FMD, and sends a Write Protected signal to the controller. Attempting to write while protected will cause a fault to be issued. The Write Protect function is enabled by a switch located on a card in the logic chassis on the MMD and FMD by a switch or switches on the operator panel on the SMD, and CMD and FMD.

CMD only - When this line is true, it indicates that the 9448 is write protected. This signal will occur during maintenance when Head Alignment is being performed, or when write protection is desired on the 9448 by depressing either of the PROTECT switches. If Write Gate becomes true when the drive is write protected on the selected volume, then the Fault line will become true. The write protected condition can be cleared by depressing the appropriate PROTECT switch.

LMD only - When this line is true, it indicates that the LMD is write protected. This signal will occur when write protection is desired by setting the PROTECT switch for the fixed volume or a tab setting on the removable volume. If Write Gate becomes true when the drive is write protected on the selected volume, then the Fault Line will become true. The write protected condition can be eliminated by resetting the PROTECT switch for the fixed volume or by changing the tab setting for the removable volume.

13. Seek End

Seek End is the combination of On Cylinder or Seek Error indicating that a Seek operation has terminated.

SMD - For a zero track seek, Seek End drops for 30 μs nominal (see Figure 8A for timing).

MMD - For a zero track seek, Seek End drops for 30 μs nominal 12/24 MB, 150 μs maximum for 80/160 MB. For a seek to fixed head cylinders, Seek End drops for 5 μs maximum (see Figures 8A and 8D for timing).

FHT MMD - For a zero track seek, this signal is derived from On Cylinder or Seek Error and drops On Cylinder for 10 μs, maximum.

CMD - For a zero track seek on the same volume, Seek End drops for 450 μs nominal. For a zero track seek with a volume change, Seek End drops for 4 ms maximum (see Figure 8B for timing). If a cylinder address greater than 822 has been selected (illegal cylinder address), Seek End will go false for approximately 450 μs.

FMD - For a zero track seek, Seek End drops for 5 ms maximum. For a seek to fixed head cylinders, Seek End drops for 5 ms maximum (see Figure 8A and D for timing).

LMD - For a zero distance seek on the same head, Seek End goes to logic 0 for 2 ms maximum. For a zero distance seek with a head change, Seek End goes to logic 0 for 10 ms maximum (see Figure 7D for timing). If a cylinder address greater than 205 has been selected (illegal cylinder address), Seek End will go false for 3 ms maximum.

In Dual Channel drives the Seek End signal sent to the unselected channel will normally be a constant one. However, if while the drive is selected on a channel, and the opposite channel receives a select, this action will be noted by circuitry within the drive. Then, when the selected channels Select and Reserve Latches are cleared, the Seek End signal sent to the waiting channel will go to a zero for 30 µs.

14. Power Sequencing (see Figures 13A thru F)

Power sequencing requires ac power on, START switch on, and REMOTE START switch (switch selectable in device) in the REMOTE position. Applying ground to the Pick and Hold lines will cause the first device in sequence to power up. Once this device is up to speed, the Pick signal is transferred to the next active device and repeated until all active devices are powered up. Individual devices may be started and stopped once power sequencing is completed.

A power failure necessitates a new power up sequence.

When in Local Start mode, each device is independently operated by its respective START switch.

In the Remote mode, a Pick or Hold is considered to be present from the controller when a ground is present on "A" cable Pin 29 for Pick and Pin 59 for Hold.

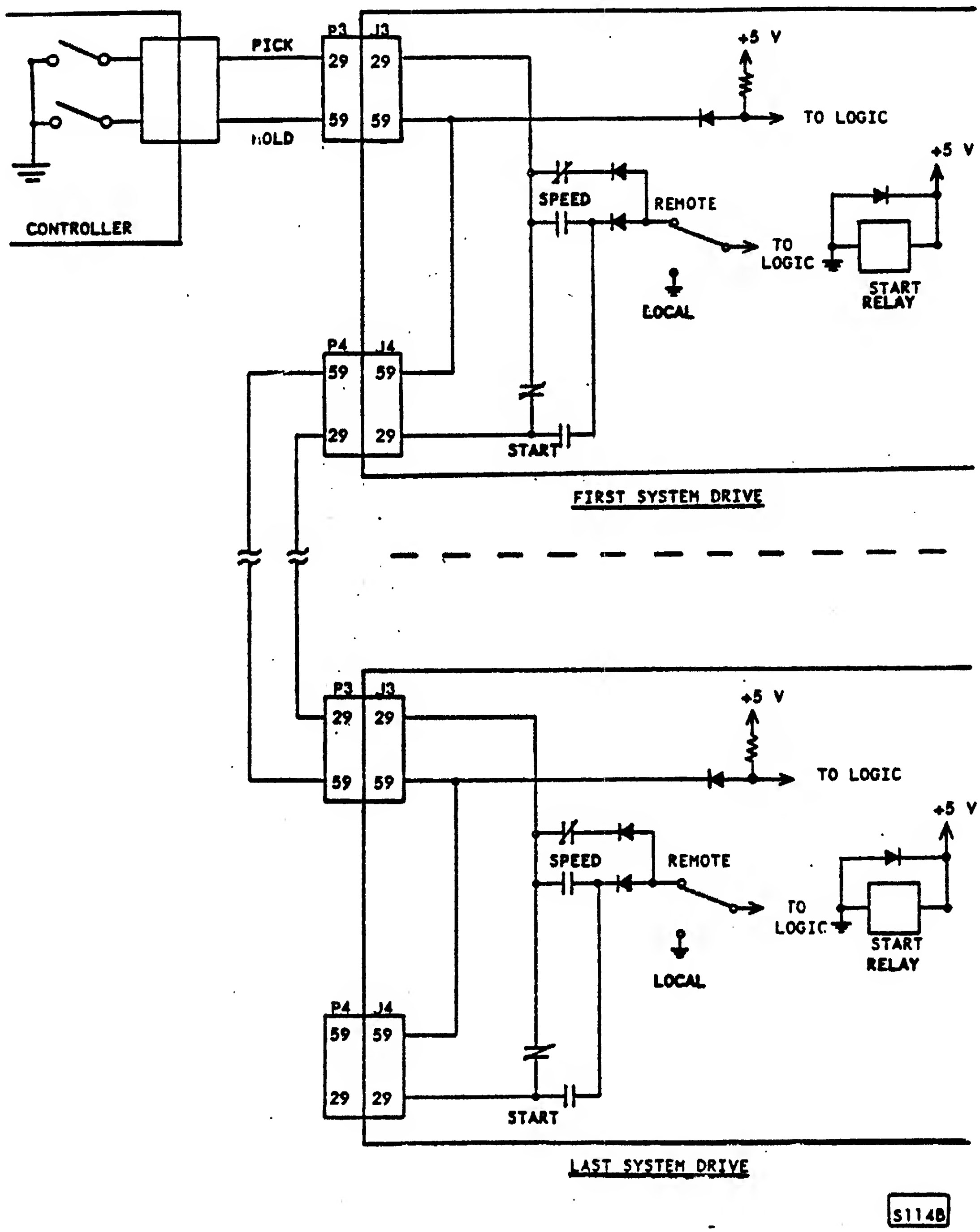


FIGURE 13A. SEQUENCE POWER LINES - MMD, FHT MMD

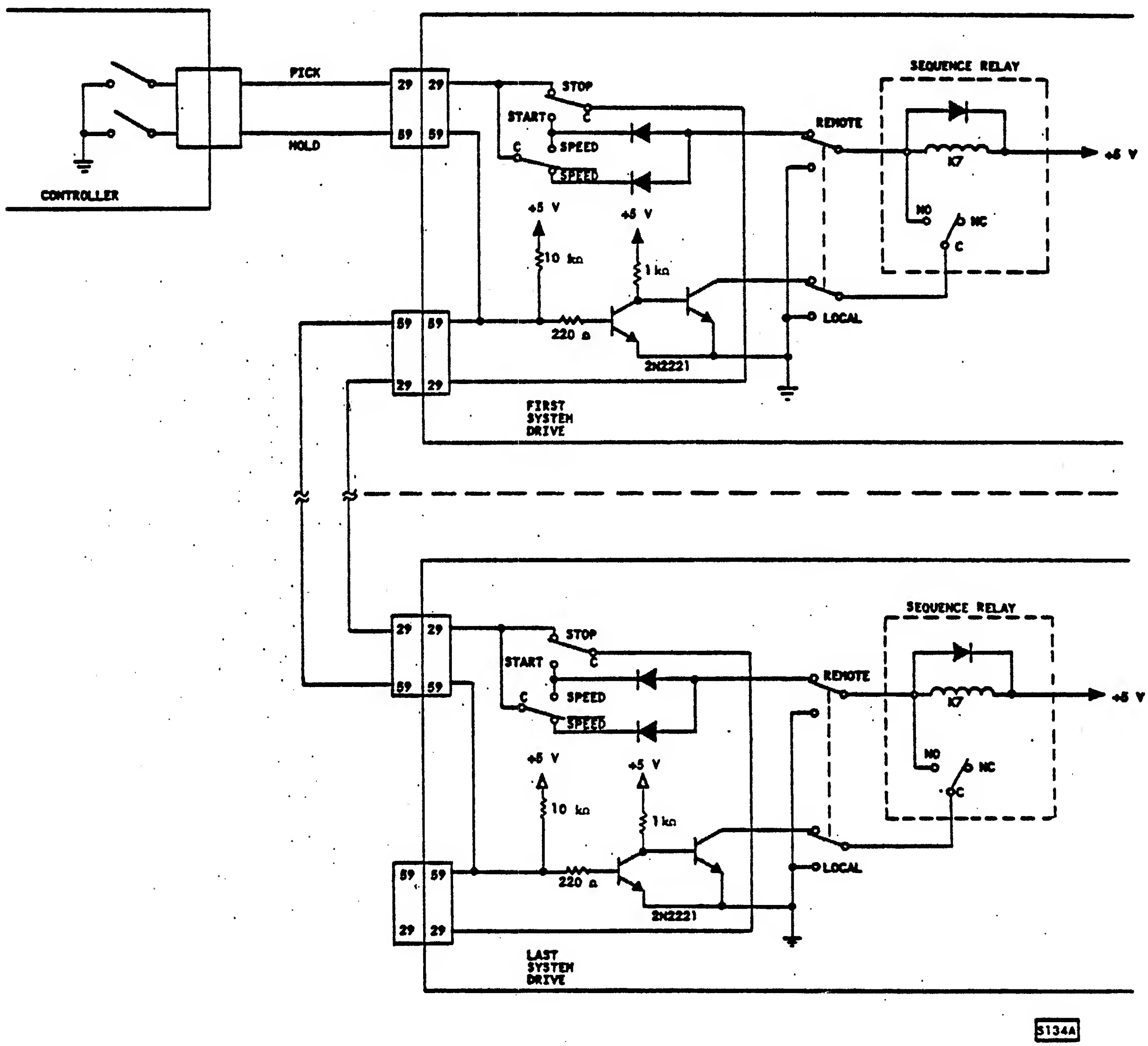


FIGURE 13B. SEQUENCE POWER LINES - 9760/9762 SMD

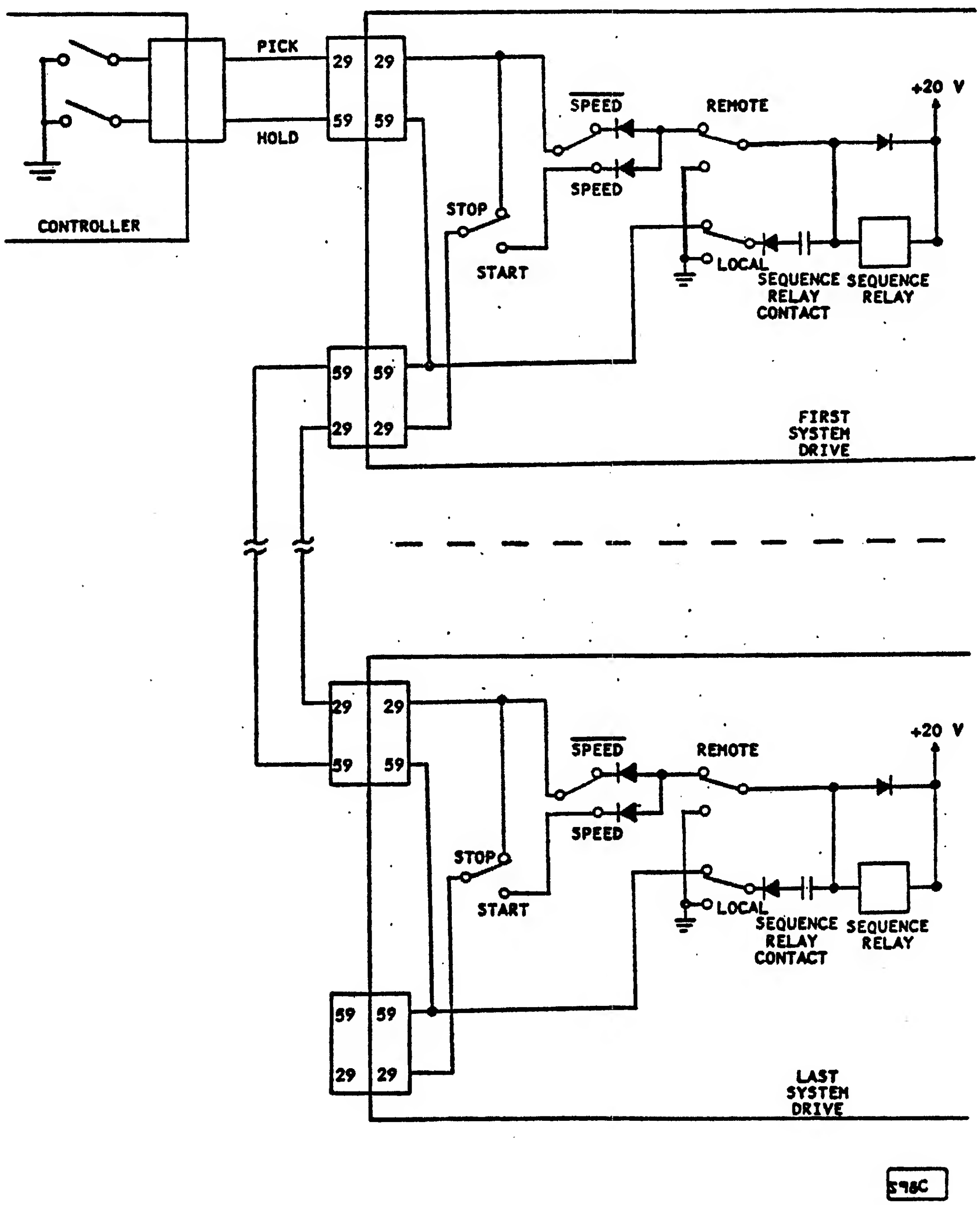


FIGURE 13C. SEQUENCE POWER LINES 9764/9766 - SMD

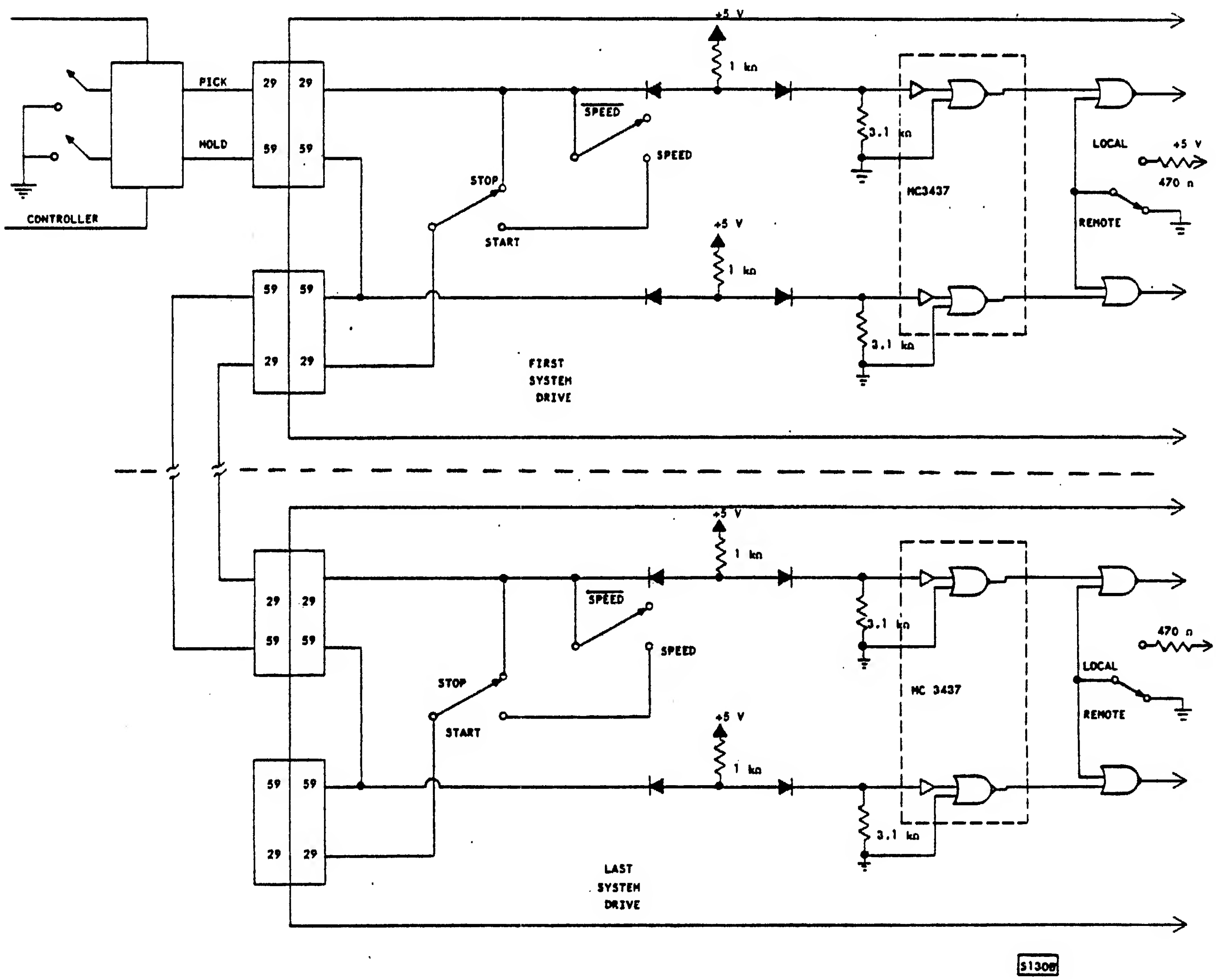


FIGURE 13D. SEQUENCE POWER LINES - CMD

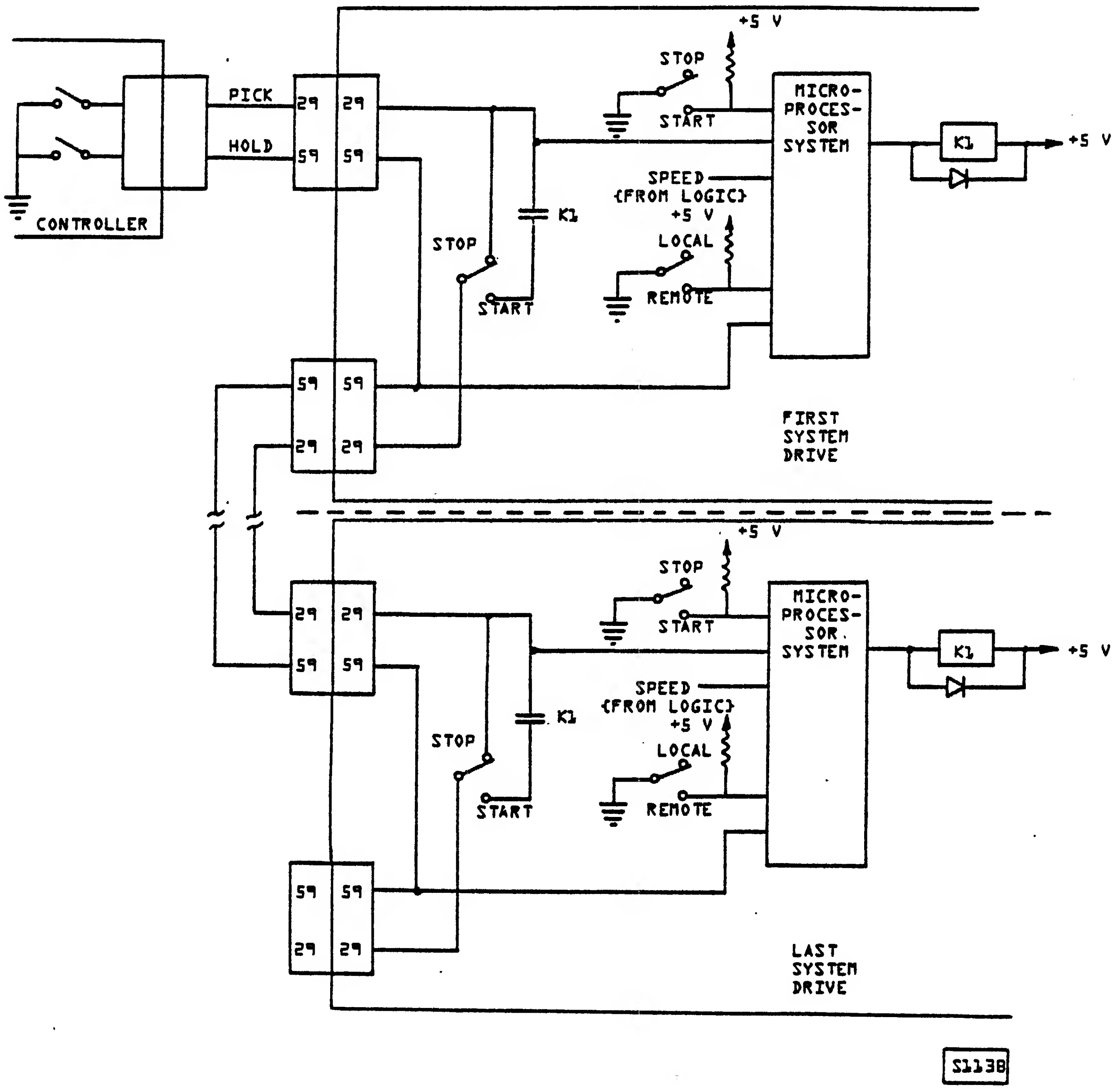


FIGURE 13E. SEQUENCE POWER LINES - FMD

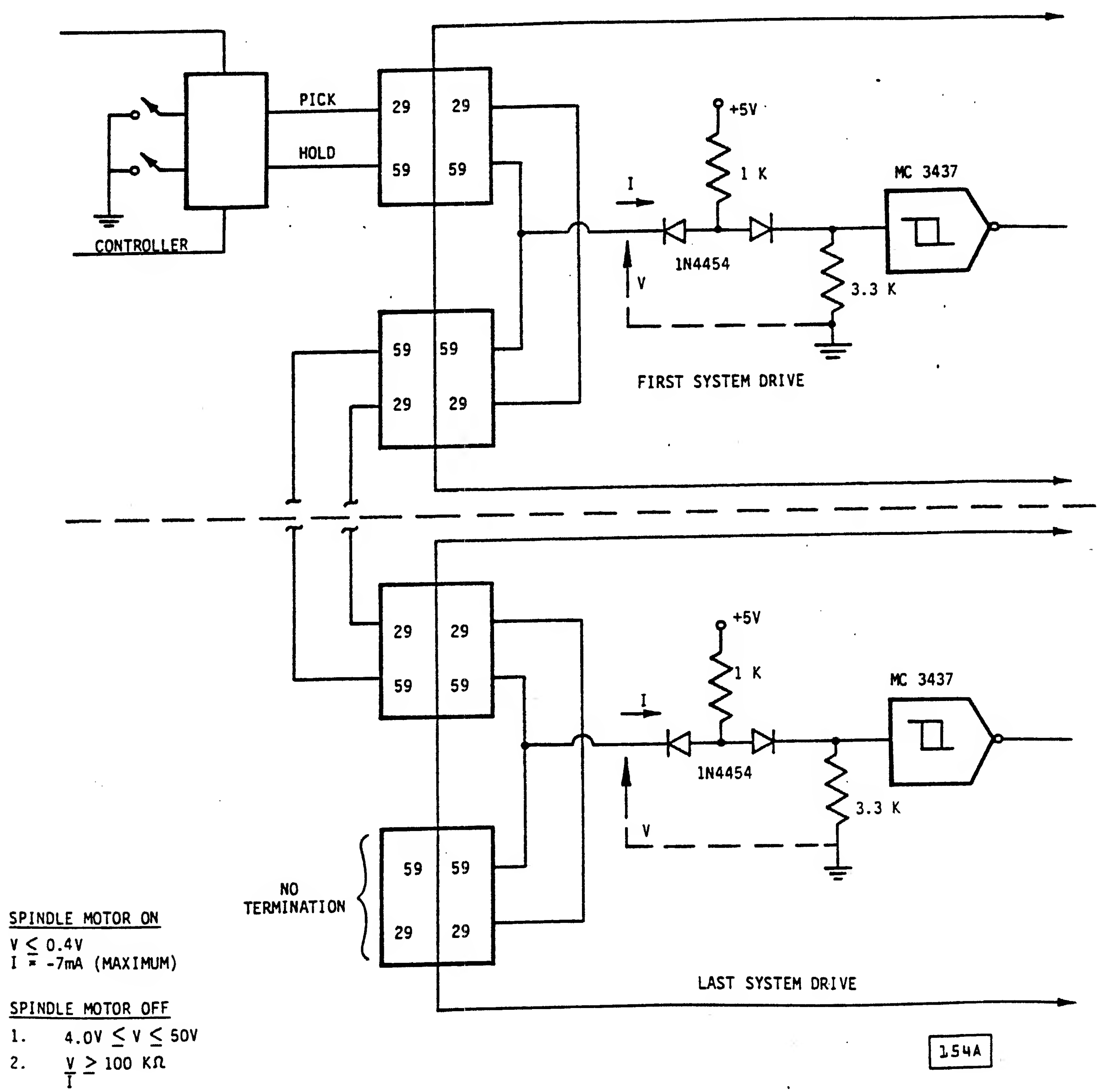


FIGURE 13F. SEQUENCE POWER LINES - LMD

Spindle Motor Control (Hold and Pick)

The Hold line enables the interface to start or stop the spindle motor provided the LMD dc power is on, the LMD ac power is on, and the control panel Start/Stop switch is in the Start position. Activation of the Hold input i.e., a logic 1 or low level will initiate rotation of the spindle motor. The spindle motor will be up to speed within 120 seconds maximum after application of the hold signal. The spindle motor up to speed condition will be reflected in the interface "Ready" line. The spindle motor may be stopped by deactivation of the Hold line (see Figure 13F). The spindle motor will be stopped within 60 seconds maximum after the Hold input is deactivated. Note the "Ready" status will go false when the Hold input is deactivated.

NOTES: The LMD will provide a 10 ms minimum noise filter to the Hold line to guard against false detection of the Hold line, due to noise.

Individual devices may be started and stopped via the control panel Start/Stop switch if the interface Hold signal is activated (Low Level or logic 1).

An internal switch is available which allows the spindle motor to be started or stopped by the control panel switch regardless of the state of the Hold input.

The LMD will directly pass the Pick signal for daisy chained opertion but will not functionally interpret this signal.

15. Busy (Dual Channel Only)

If the device is already reserved and/or selected, a Busy signal will be issued to the "A" cable and Unit Selected will be issued on the "B" cable to the channel attempting the select. This Busy signal will be issued from the device at its I/O connector within 600 ns following the selection attempt, and will remain at this status until Unit Select Tag is dropped or the unit is no longer Busy. Unit Selected should be used to enable Busy in the controller (see Figure 12 for timing).

NOTE: The CMD has no Dual Channel option.

The LMD has no Dual Channel option, but this signal is daisy chained, at the connector. This signal output is electrically undefined for a LMD with no electrical connections made within the LMD except a daisy chain connection at the connectors.

5.2.3 Data and Clock Lines

1. Write Data

This line carries data which is to be recorded on the disk pack.

2. Servo Clock

The Servo Clock is a phase-locked 9.677 MHz clock generated from the servo track quadbits on the MMD, and dibits on the SMD and CMD. This phase-locked clock (see Figure 14) is used to generate write data. Servo Clock is available at all times (not gated with Unit Select). For CMD, Servo Clock is rephased at a volume change (see Figure 18).

LMD - This clock is frequency locked to the disk rotational speed by sampling a field within the embedded servo. Since the Servo Clock is derived via a sampled PLO system, the exact number of servo clocks between sector pulses may vary by ±4 clock cycles.

3. Read Data

This line transmits the recovered data in the NRZ form (see Figure 14).

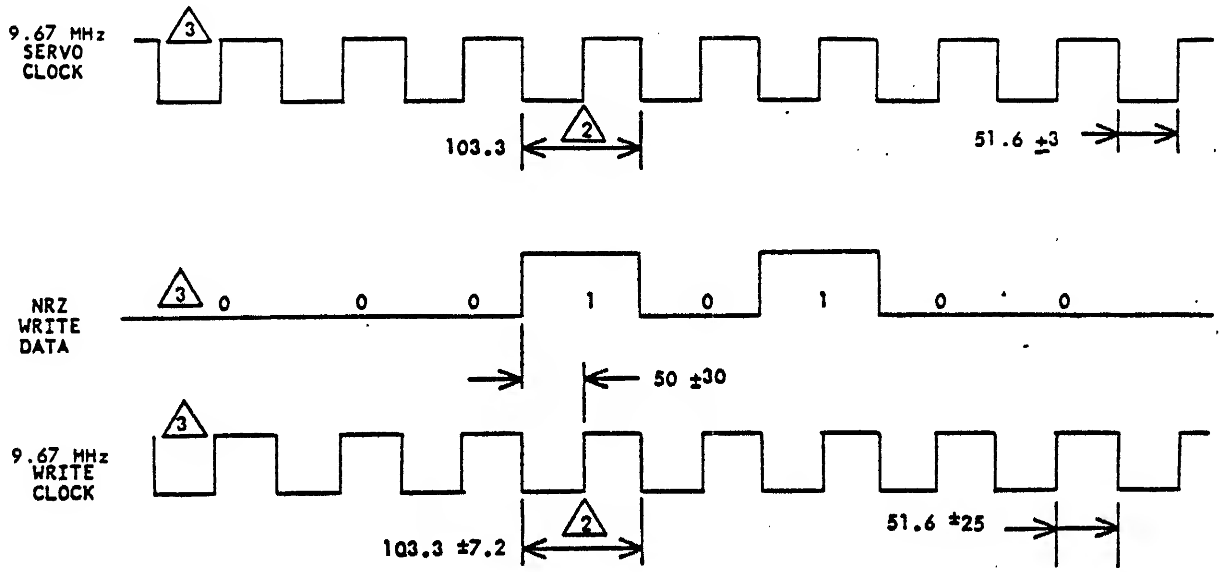
4. Read Clock

The Read Clock defines the beginning of a data cell. It is an internally derived clock signal and is synchronous with the detected data as specified in Figure 14. This signal is transmitted continuously, and is in phase sync within 9 μs after Read Gate.

LMD - This signal is in phase sync within 88 servo clock periods from the concurrence of Read Gate and a PLO sync field.

5. Write Clock

This line transmits the Write Clock signal which must be synchronized to the NRZ data as illustrated in Figure 14. The Write Clock is the Servo Clock retransmitted to the device during a Write operation. The Write Clock need not be transmitted continuously, but must be transmitted at least 250 ns prior to Write Enable, or Write Gate.



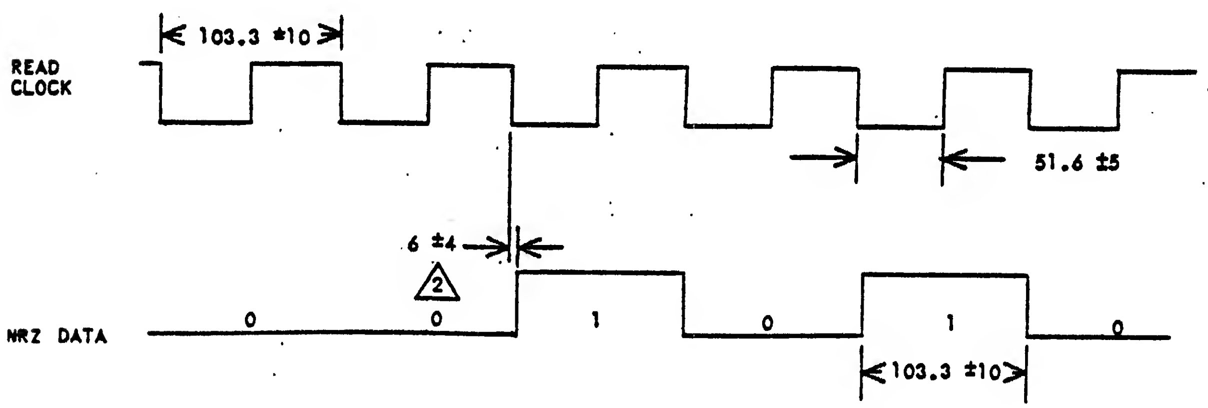
NOTES:

1 ALL TIMES IN ns.

2 SIMILAR PERIOD SYMMETRY SHALL BE ±2 ns. AT I/O CONNECTOR IN DRIVE, SPEED VARIATION TOLERANCE SHALL BE -5%, +4% OF PERIOD WHICH INCLUDES SPINDLE SPEED TOLERANCE AND DIBIT DROPOUT WHILE CARRIAGE IS MOVING.

LMD - EXCEPT DURING A HEAD CHANGE OR PLO SYNCHRONIZATION THE CLOCK VARIANCES FOR SPINDLE SPEED AND CIRCUIT TOLERANCES SHALL NOT VARY MORE THAN - 5.5% TO +4%.

3 AT I/O CONNECTOR IN CONTROLLER.



NOTES:

1 ALL TIMES IN ns.

2 NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

M530A

FIGURE 14. NRZ DATA AND READ CLOCK TIMING

5.3 Data Format and Data Control Timing

The Record Format on the disk is under control of the controller (LMD only - The Record Format on the disk is under limited control of the Controller; i.e., the embedded servo field may not be modified by the Controller). The Index and Sector pulses are available for use by the controller to indicate the beginning of a track or sector. Suggested formats for fixed and variable sector data records are shown in Figures 15A, B and C.

Some hardware-oriented constraints must be recognized when designing a format. The following is a list of those format parameters:

1. Read Initialization Time

   All except LMD - Between the deselection of one head and the selection of another head, there is a 5.0 µs delay within the device due to circuit characteristics. The time from the initiation of a head change until data can be read with a selected head without error, is 24.0 µs, maximum (5.0 µs for head selection, and 10 µs for read amplifier stabilization and 9.0 µs for phase lock synchronization).

   LMD - The maximum time until data can be read from a newly selected head is 10 ms.

2. Write-to-Read Recovery Time

   Assuming a write operation is in progress, the time lapse before Read Gate can be enabled after switching the Write Gate off is 10 µs, minimum.

3. Read-to-Write Recovery Time

   Assuming a read operation is in progress, the time lapse from dropping Read Gate to enabling Write Gate shall be 0.3 µs, minimum (see Figures 9A and B).

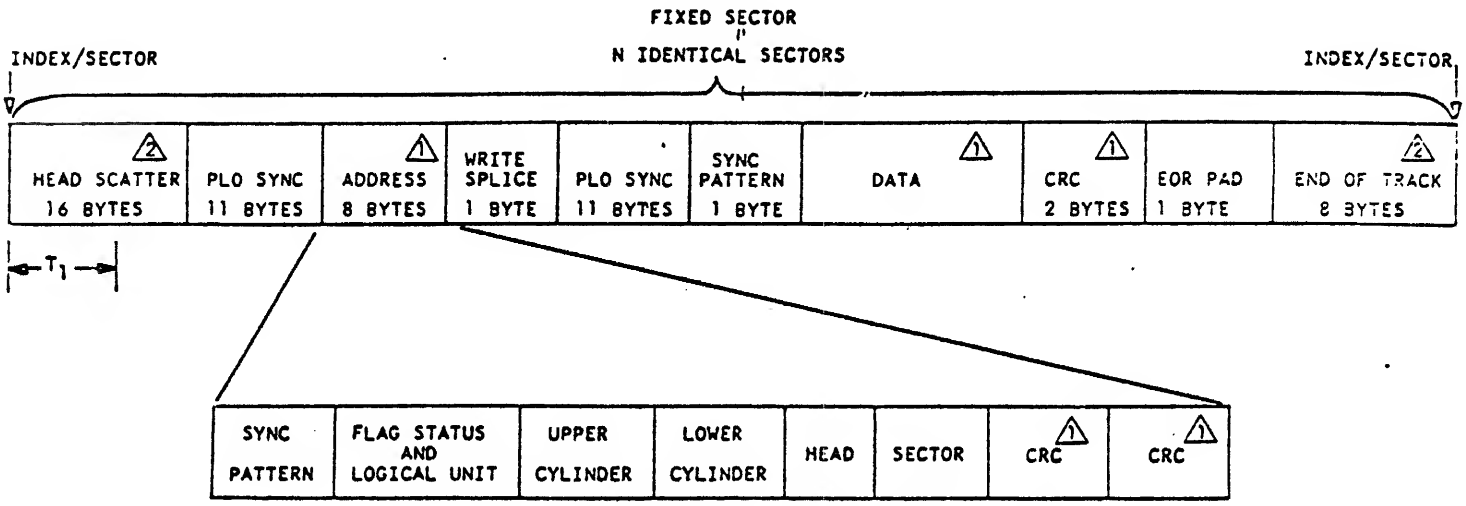
4. Beginning-of-Record Tolerance (See Notes on Figures 15A and B)

   This tolerance must be provided to allow for worst case conditions of head skew and circuit tolerances.

   This gap must be written with a minimum of 16 bytes of zeros.

5. Read PLO Synchronization

   The synchronization time needed to allow the Phase-Locked Oscillator to synchronize is 9 µs of zeros.



T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

D135C

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

$$\text{DATA FIELD} = \frac{20\ 160}{64} - 59 = 256\ \frac{\text{BYTES}}{\text{SECTOR}}$$

DATA = 256 BYTES/SECTOR

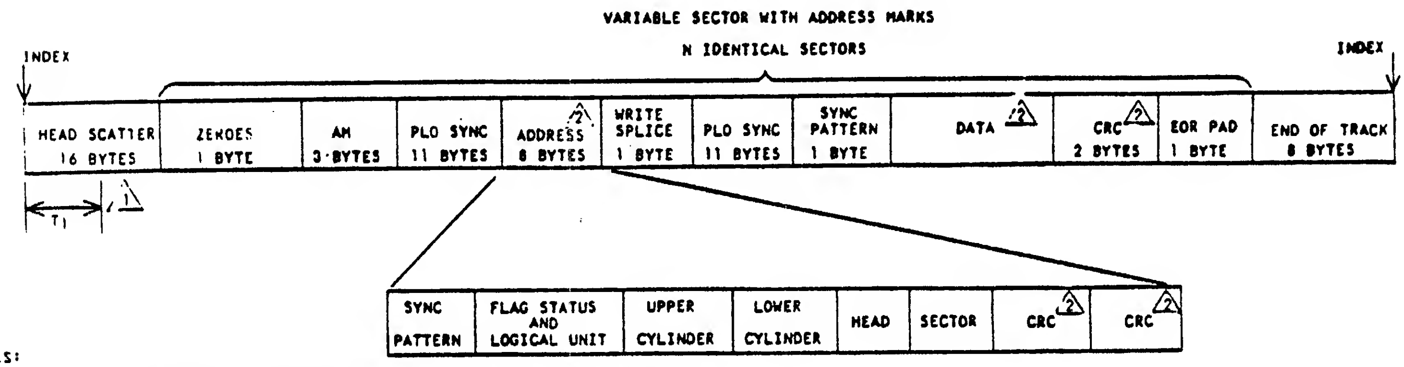
$$\text{\% EFFICIENCY} = \frac{256 \times 64}{20\ 160} \times 100 = 81\%$$

NOTES:

△1 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

△2 NOT REQUIRED IN MMD FORMAT SHOWN ONLY FOR SMD FAMILY COMMONALITY. THESE GAPS SHOULD BE PADDED WITH SUFFICIENT BYTES TO ALLOW FOR CYLINDER AND HEAD SWITCHING TIMES AT INDEX OR SECTOR TIMES.

FIGURE 15A. SECTOR FORMAT - FIXED



NOTES:

1. T_1 = TIME BETWEEN LEADING EDGE OF INDEX AND READ GATE IS 8 BYTES. A SPLICE POINT MAY EXIST WITHIN THIS AREA.
2. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

D136D

EXAMPLE NO. 1: WHAT IS DATA FIELD LENGTH USING 64 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK} - \text{MECHANICAL TOLERANCES}}{\text{NUMBER OF SECTORS/TRACK}} - (\text{SYNC FIELDS AND ADDRESS})$$

$$\text{DATA FIELD} = \frac{20\,160\ \frac{\text{BYTES}}{\text{TRACK}} - 24\ \frac{\text{BYTES}}{\text{TRACK}}}{64\ \frac{\text{SECTORS}}{\text{TRACK}}} - 39\ \frac{\text{BYTES}}{\text{SECTOR}} = 275\ \frac{\text{BYTES}}{\text{SECTOR}}$$

$$\%\ \text{EFFICIENCY} = \frac{275 \times 64}{20\,160} \times 100 = 87\%$$

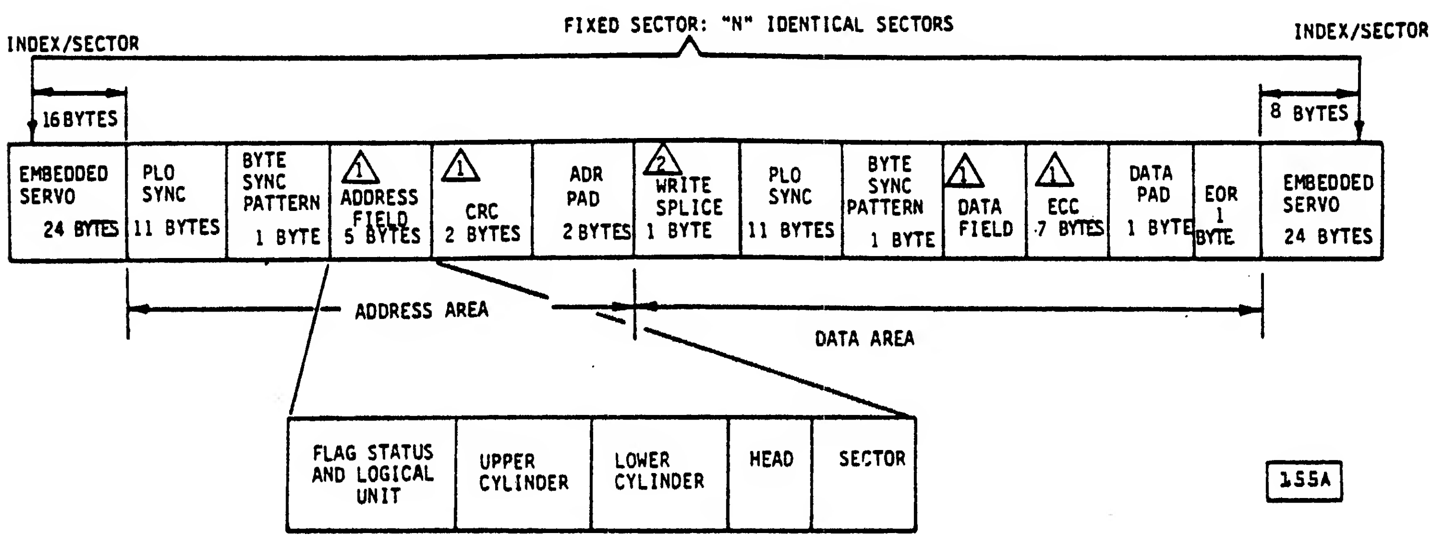
EXAMPLE NO. 2: WHAT IS NUMBER OF SECTORS USING 256 DATA BYTES?

$$\text{N SECTORS} \quad \frac{20\,160 - 24}{256 + 39} = 68 \text{ SECTORS}$$

$$\%\ \text{EFFICIENCY} = \frac{256 \times 68}{20\,160} \times 100 = 86\%$$

I.136D

FIGURE 15B. SECTOR FORMAT - VARIABLE



EXAMPLE NO. 1: DATA FIELD LENGTH USING 64 SECTORS

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

$$\text{DATA FIELD} = \frac{20{,}672}{64} - 67$$

DATA = 256 BYTES/SECTOR

$$\text{\% EFFICIENCY} = \frac{256 \times 64}{20{,}672} = 79\%$$

△1 THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

△2 THIS WRITE SPLICE BYTE IS IN THIS LOCATION AS A RESULT OF A RECORD UPDATE. FOR FORMATTING CONSIDERATIONS THIS BYTE MAY BE ALLOWED FOR AT THE END OF THE DATA SECTOR BY INCREASING THE NUMBER OF EOR (END OF RECORD) BYTES FROM 1 TO 2. (REFER TO SECTIONS 4.1 AND 4.2)

FIGURE 15C. SECTOR FORMAT, LMD

6. Sync Pattern

The Sync Pattern consists of "1" bits indicating the beginning of the address or data area (one "1" bit is the minimum required).

7. Write Driver Turn On

The Write Driver Turn On time is about 0.8 μs or one byte. This time has to be accounted for in order to know where possible splice areas are located.

8. End-of-Record Tolerance (See notes on Figures 15A and B)

This tolerance is an eight byte pad of zeros which eliminates the possibility of destroying the end of a record written with a later displacement head.

LMD ONLY - The Format presented in Figure 15C consists of three functional areas: Embedded Servo, Address, and Data. The Data area is used to record the system's data files. The Address area is used to locate and verify the track and sector location on the Disk where the Data areas are to be recorded.

a. Embedded Servo Area

This area is 24 bytes long and is permanently preformatted on each track, it contains information for the drive's positional servo logic. This area is used solely by the drive and is not accessible by the controller, although the controller must allow for its existence.

NOTE: The LMD will internally ignore Read or Write Gate during the Embedded Servo Area.

This gap also serves as an interrecord gap between sectors to allow Controller decision making time.

b. Address Area (Figure 15C)

The address area is used to provide a positive indication of the track and sector locations. The address area is normally read by the Controller and the address bytes verified prior to a data area read or write. The address area is normally only written by the Controller during a format function (Section 5.3.1) and thereafter only read to provide a positive indication of the sector location and establish the boundaries of data area. The address area consists of the following bytes.

- PLO Sync (11 bytes minimum)

  These 11 bytes of zeros are required by the drive to allow the drive's read data phase locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

- Byte Sync Pattern (1 byte)

  This byte is user-defined; it indicates to the user's Controller the beginning of the address field information, and it establishes byte synchronization (i.e., the ability to partition this ensuing serial bit stream into meaningful information groupings, such as bytes).

- Address Field

  These bytes are user-defined and interpreted by the user's Controller. A suggested format consists of five bytes, which allows one byte to define flag status bits or logical unit number, two bytes to define the cylinder address, one byte to define the head address and one byte to define the sector address. (Although one byte of cylinder address encompasses the current LMD cylinder address space, two bytes are suggested for future enhancements and/or "module drive" family compatibility).

- CRC (2 bytes recommended) - (Address Field Check Codes)

  Selection of an appropriate error detection mechanism, such as a cyclic redundancy check code, is made by the user and applied to the address for file integrity purposes. These codes are generated by the user's Controller and written on the media when the address field is written. Data integrity is maintained, by the user's controller recalculating and verifying the address field check codes when the address field is read.

- ADR Pad (2 bytes) - (Address field pad)0
  The Address Field Pad bytes must be written by the Controller and is required by the drive to ensure proper recording and recovery of the last bits of the address field check codes.

c. Data Area (Figure 15C)

The data area is used to record the user's data fields. The contents of the data fields within the data area are usually specified by the Host Computer system. The remaining parts of the data area are usually specified and interpreted by the user's disk controller to recover the data fields and ensure their integrity. The data area consists of:

- Write Splice (1 byte)

  This byte area is required by the drive to allow time for the write drivers to turn on and reach a recording amplitude sufficient to ensure data recovery. This byte should be allowed for in the format is described in greater detail in Section 5.3.2.

- PLO Sync (11 bytes)

  These 11 bytes of zeros are required when reading to allow the drive's phase locked oscillator to become phase and frequency synchronized with the data bits recorded on the media.

- Byte Sync Pattern (1 byte)

  This byte is user defined and indicates to the user's controller the beginning of the data field bytes plus establishes byte synchronization for the data field.

- Data Field (256 bytes with 64 sectors per track, or 512 bytes with 32 sectors per track)

  The data field contains the Host System's data files.

- ECC (7 bytes maximum - (Data Field Check Codes)

  Error correction codes are user defined and provide error detection and correction capability on the data field. The use of ECC is recommended for the LMD but is not mandatory.

- Data Pad (1 Byte) - (Data Field Pad)

  The Data Field Pad byte must be written by the Controller and is required by the drive to ensure proper recording and recovery of the last bits of the data field check codes.

- End of Range (1 byte)

  This byte is required by the drive to account for electro-mechanical tolerances. They are not necessarily read or written, but they must be allocated in the sector format design.

The sector format in Figure 15C has been defined to account for restrictions placed on the format by the drive as well as functionality required by a disk controller. The following two sections recommend a procedure to be followed by the controller in order to format media per this format (Section 5.3.2) and discuss the control timing required to perform a data field read function and a data field write function per this format (Section 5.3.3).

5.3.1 Write Format Procedures

1. Procedure for SMD, MMD, FHT MMD, CMD, FMD

Provisions must be made within the controller to format the disk. The following procedure is recommended for fixed sector formats:

a. Select desired unit, cylinder, volume (CMD only), head and sector.

b. The controller must provide a 5 µs minimum delay between selec- ting a head and initiating a search for leading edge of sec- tor. This delay will ensure that the unit will be ready to write when the sector leading edge is detected.

c. Search for leading edge of desired sector.

d. Detect leading edge of selected sector and bring up Write Gate and start writing zeros.

e. Write all zeros for head scatter and PLO Sync areas (27 bytes).

f. Write a sync pattern, the address, and the address checkword.

g. Write all zeros for Write Splice gap and PLO Sync field (12 bytes).

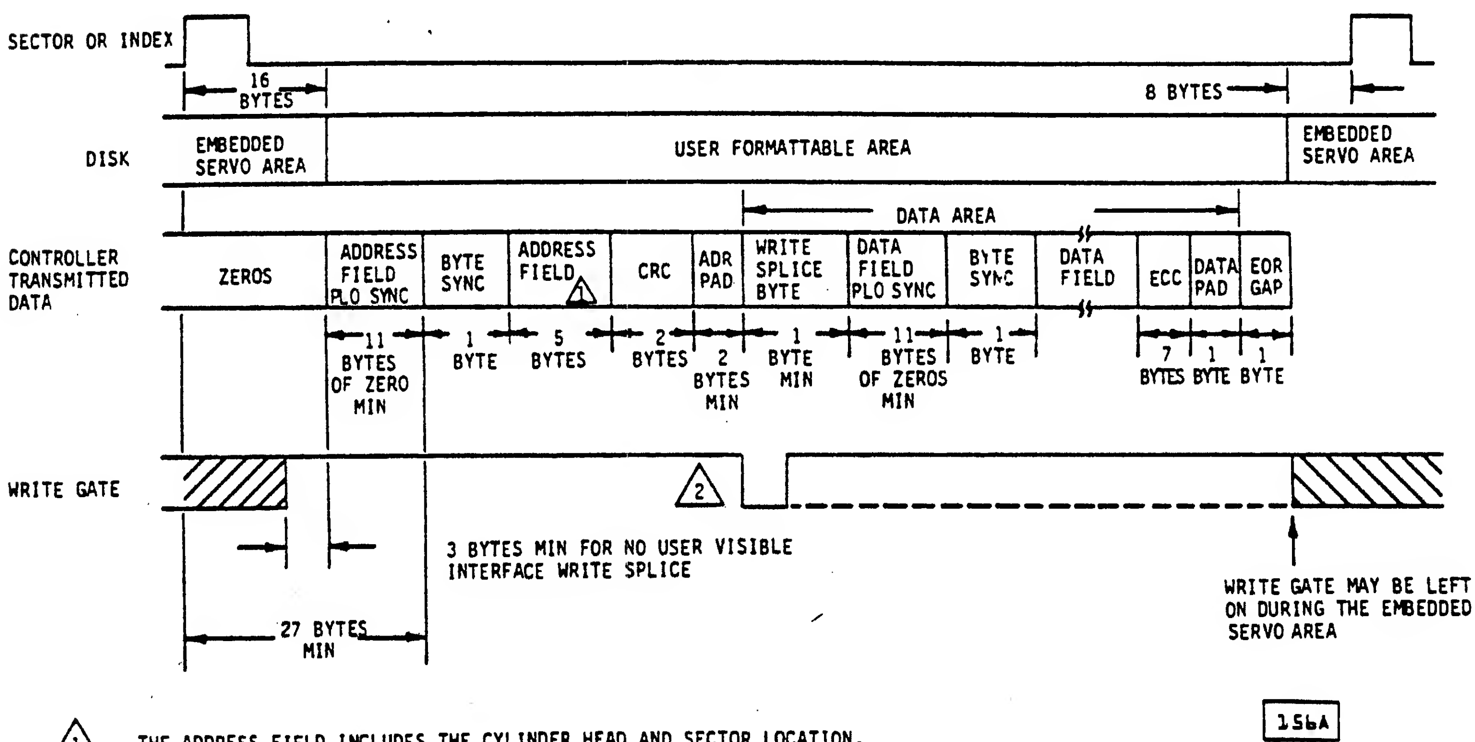
h. Write a sync pattern, the data field, the two byte data field checkword, and the one byte pad. The data field should prefer- ably be a worst case pattern.

i. The end tolerance gap is the only part of the format where there may be erased areas with no write data. If erased areas occur in Gap 2 there may be problems in recovering the data following this gap. It is preferable to write zeros to the next sector pulse.

j. If the next sector of the same track is to be formatted and the head is not deselected, the Write Gate should be left on. In this case, the controller should write all zeros in the toler- ance gap. If Write Gate is dropped, it should not be raised again within 2 µs.

2. Procedure for LMD

Provisions must be made within the Controller to format the disk. The following procedure is recommended for fixed sector formats with separate address and data fields (See Figure 16).



1 THE ADDRESS FIELD INCLUDES THE CYLINDER HEAD AND SECTOR LOCATION.

2 WRITING THE DATA AREAS ARE OPTIONAL. THESE AREAS ARE USEFUL TO VERIFY THE INTERGRITY OF THE SECTOR IF THE FORMATTER READ VERIFIES THESE AREAS AFTER A FORMAT OPERATION WHICH ALSO WRITES THE DATA AREAS.
IF DATA FIELDS ARE TO BE WRITTEN, WRITE GATE MUST BE DEACTIVATED FOR A MINIMUM OF ONE BIT TIME AFTER THE ADDRESS PAD AND REACTIVATED 6 BITS PRIOR TO THE DATA FIELD PLO SYNC AREA.

FIGURE 16. FORMAT TIMING, LMD

Procedure (see Figure 18

a. Select desired unit, cylinder, volume and head.

b. The Controller must wait for "On Cylinder" to begin a search for the leading edge of Index. This wait period will insure that the unit will be ready to write when the leading edge of Index is detected plus insure rotational position integrity as defined by the Index and Sector pulses.

c. Search for the leading edge of desired Sector pulse.

NOTE: The Index pulse provides a common rotational reference for each track and is considered a sector pulse.

d. Detect the leading edge of the selected Sector pulse and activate Write Gate and start transmitting zeros.

NOTE: The embedded servo is a write protected area (by the drive) and data transmitted to the drive by the Controller during the embedded servo time will not be written on the disk; however, to control write splice timing between the embedded servo area and the address PLO Sync field it is recommended that the controller activate Write Gate and begin transmitting all zeros no later than 13 byte times after the leading edge of the Sector pulse.

e. Transmit all zeros during the embedded servo area (beginning at least three byte times before the end of the embedded servo area) and for the address PLO sync field (11 bytes minimum). This is equivalent to transmitting a minimum of 27 bytes of zeros from the leading edge of the Sector pulse.

f. Transmit a byte sync pattern, the address field, and the address field check codes (CRC).

g. Transmit all zeros for the address field pad bytes, and terminate the Write Gate.

h. If a data field is to be written, proceed to Step 9, if no data field is to be written, proceed to Step 11.

i. Reinitiate Write Gate during the write splice byte. Transmit all zeros for a data field PLO sync area (11 bytes minimum), transmit a data field byte sync pattern, the desired data, and the data field check codes (ECC).

j. Transmit all zeros for the data field pad (1 byte minimum)

k. The controller may now terminate the write function and proceed to Step 1 if the entire track has been formatted or proceed to Step 3 if additional sectors on this track to be formatted. If additional sectors on the track are to be formatted, the Controller may leave Write Gate on until the next Sector pulse is detected and then proceed to Step 4. (If sequential sectors are to be formatted, Write Gate may be continuously left on, but the controller timing must be reinitialized with the next Sector pulse.)

This format procedure has allowed three bytes between the last bit of the address field check code and the first bit of the data field PLO sync field (i.e., the Address Field Pad and the Write splice bytes). However, if during formatting, Write Gate is enabled relative to the Sector pulses and the address and data areas are written consecutively (i.e., no physical write splice is created between the address and data areas), then only the Address Field Pad byte is required if three End of Range (EOR) bytes are allowed for at the the end of the data area. (This allows CMD family format routines to be used for the LMD with a different number of format bytes only required between the end of the data field and the next sector pulse). Note that this format variation is still compatible with the normal read/write routines since a splice will be created per Figure 14C when a record update function is performed, redistributing the 3 byte EOR to a 1 byte EOR field and a write splice byte.

5.3.2 Control Timing (See Figures 9A and B) (All Drives Except LMD)

1. Read

The control line associated with a Read command is the Read Gate line.

The leading edge of Read Gate forces the Phase Locked Oscillator to synchronize on all zeros pattern. Read Gate also enables the output of the Data Separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ±4 clock counts after the leading edge of Index or Sector.

The Sync Pattern search may begin 88 Servo Clock counts after the leading edge of Read Gate, or after the trailing edge of Address Mark Found.

Head switching and read amplifier stabilization (see Figure 9A and B) shows the latest acceptable time at which a head can be selected in order to read the next successive sector (with the format described in 5.3).

Data I/O lines may not have valid data until 9 µs from leading edge of Read Gate, due to phase lock synchronizing time.

There should be no splice area after Read Gate is brought up.

2. Write Data Field

The control line associated with a Write operation is Write Gate.

The Sector Address must always be read and verified prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the PLO Sync field and Sync Pattern.

The controller must provide a three bit internal delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal (see Figure 9A and B). This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

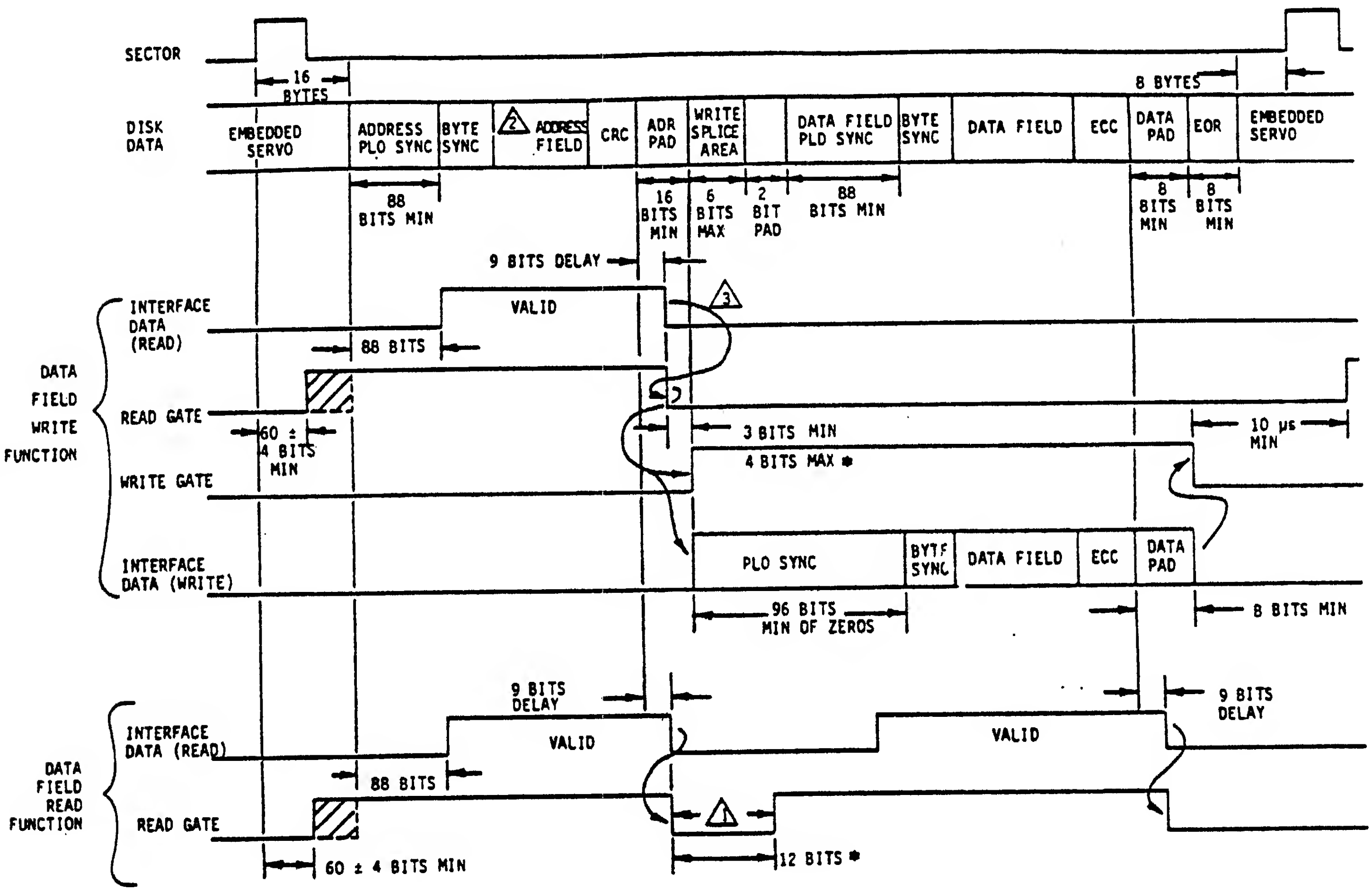
Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised upon sensing Index or Sector. During a record update, Write Gate is raised within two bits of the last bit of an address, but no closer than 1 bit.

5.3.3 Read/Write Control Timing (see Figure 17 LMD)

The objective of this section is to specify the interrelationship of the drive interface control leads necessary to recover or record data fields on a formatted disk media. The format of Section 5.3.1 will be assumed; however, critical drive dependent parameters will be summarized to enable controller variations in the read/write timing.

To perform a data field read function, the address field is read and verified, then its data field is read. To perform a data field write function, the address field is read and verified, then the data area is written. The following sections will expand on these concepts.



1 READ GATE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD. THE 12 BYTE EXAMPLE CONSISTS OF ONE BYTE OF WRITE SPLICE AND 11 BYTES FOR PLO SYNC.

2 THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.

3 CABLE/CONTROLLER DELAY NOT SHOWN. MUST BE ≤ 4 BIT TIMES FOR THIS EXAMPLE. ALL TIMING SPECIFIED AT THE DRIVE CONNECTOR.

* VALUES ARE FOR THIS EXAMPLE.

157A

FIGURE 17. TYPICAL READ/WRITE TIMING LARK

The LMD read function consists of reading the address fields and then the data fields. The critical interface lines associated with a read function are the Sector (Index pulses, Read Gate, Read Clock, Read Data, and Servo Clock lines.

Address Field Read (see Figure 17). The location of the address field is defined relative to the Sector (Index) pulse. To recover the address field the Controller waits for the leading edge of a Sector (Index) pulse. 60 ±4 Servo clock periods after the leading edge of a Sector (or Index) pulse Read Gate may be activated. The leading edge of Read Gate forces the phase locked oscillator to synchronize on the PLO sync field. Read Gate also enables the read data output of the data separator after frequency and phase synchronization is established. Synchronization to the PLO sync pattern will not begin until the end of the embedded servo area with internal drive logic accounting for the write splice between the embedded servo and the address field PLO sync if the formatter initiated a sector format function at least 3 bytes prior to the end of the embedded servo area.

Read Data will be valid within 88 Servo Clock periods after the concurrence of Read Gate and the PLO sync field. Read Clocks are transmitted continuously and will be in phase and frequency synchronization with the Read Data within 88 Servo Clock periods after the concurrence of Read Gate and the PLO sync field. The Read Data lines will be a logic zero until the first one bit of the byte sync pattern is detected. It is then the controllers responsibility to establish byte synchronization, perform the address field verification and interpret the address field check codes (CRC). Read Gate may be deactivated after the last bit of the address field check code is received by the Controller and must be deactivated at least one bit prior to a Write Splice area.

For example, consider the format of Figure 17. This example has a Write Splice area located on the disk two bytes after the address field check codes (the creation of this Write Splice area will be explained in Section 5.3.3.2). An examination of the Interface Data (Read) timing signal of Figure 17 reveals that the Interface Read Data is delayed by 9 bit times from data recorded on the media. Thus, to meet the requirement that Read Gate must be deactivated at least one bit prior to a Write Splice area requires that, for the format of Figure 17, Read Gate must be deactivated within six bit times after the reception of the last bit of the address field check code by the controller.

Summary of Critical Read Function Timing Parameters

Controller variations of the read timing are allowed if the following drive-dependent parameters are met;

1. Read Initialization Time

   Any head command requires a seek, and a read or write may not be initiated until On Cylinder is true following the seek command for the head change.

2. Read Gate Timing

   Requesting the drive to establish bit synchronization (i.e., enabling Read Gate) for the address area should be done no earlier than 60 ±4 bits from the leading edge of a Sector (Index) pulse and at least 11 bytes prior to the address field byte sync pattern.

   Read Gate may not be enabled or True during a Write Splice area (Read Gate must be deactivated one bit time minimum before a Write Splice area and may be enabled one bit time minimum after a Write Splice area).

   NOTE: Data (Read) at the interface is delayed by 9 bit times from the data recorded on the disk media.

The Controller may compare the contents of the disk media recorded address field to the desired sector location as they are received from the drive. However, a valid comparison should not be assumed until the disk media recorded CRC check code verifies its correctness. If the recorded and desired address fields compare and no check code error is detected, then the desired Data Area for either a data field update or data field read function has been found.

Data Field Read (see Figure 17)

After the desired sector location has been found by comparison to the address field, the data field may be read. When a data field is updated a 6 bit wide Write Splice area is created on the media (see Section 5.3.3.2). Read Gate must be deactivated a minimum of one bit time preceding a Write Splice area and may be activated a minimum of one bit after a Write Splice area. For example consider the format of Figure 17. To satisfy the Read Gate/Write Splice timing requirements, Read Gate could be deactivated as soon as the last bit of the Address Field check code was received by the controller and activated 12 bit times following the Write Splice area.

The example chose to deactivate Read Gate as soon as the last bit of the address field check code was received (versus deactivating Read Gate 6 bit times after the last bit of the address field check code) for timing compatibility with the data field update function (Section 5.3.3.2) which assumed this timing relationship to enable Write Gate and create the Write Splice area in the location shown in Figure 17.

Per Figure 17 if the Read Gate is activated after the Write Splice and at the beginning of the Data Field PLO Sync area, the interface Read Data lines will be valid within 88 servo clock periods. (The two bit pad following the Write Splice area allows Read Gate to be activated a minimum of 1 bit time after the Write Splice and still insures 11 bytes of Data Field PLO Sync Characters). The Controller may then search for the Data field byte sync pattern, establish byte synchronization, and read the Data field plus read and intrepret the Data field check codes. Read Gate may be deactivated after the last bit of the data field check code (ECC) is received (i.e., after the required number of Read Clocks is received after byte synchronization is established.

Write Function (Figure 17) LMD.

The Write function consists of reading the address field to verify the sector location, and then writing the Data Area PLO Sync characters, the Byte Sync pattern, the Data Field the Data Field Check Codes (ECC) and a Data Field Pad byte. The critical interface lines associated with the write function are the Write Gate, Write Data, and Servo Clock lines.

Read Address Field Prior To Write.

The address field and address field check codes should be read and verified prior to writing the data area, except while formatting.

Write Splice Creation

The last interface Read Data bit of the address field check codes will be delayed by 9 bit times from the recorded disk location. Thus if the Controller deactivates Read Gate when the last bit of the address field check code is detected, the disk R/W head will be located 9 bit times into the address pad byte. When the Read gate is deactivated the Write clocks to the drive should be enabled. (The Drive requires Write clocks to precede Write Gate by a minimum of 250 ns).

The Controller must provide three-servo clock periods, minimum, of delay (approximately 0.3 µs) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal. This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit. This from Figure 17, if the Read Gate was deactivated when the last interface data bit of the address field check code was received by the Controller and the Write Gate was activated 4 Servo Clock periods after Read Gate was deactivated a Write Splice area would be created at the location shown in Figure 17 (i.e., the Write Splice area on the media would start 16 bit times from the last bit of the recorded address field check code). In addition, if Write Clocks were enabled when Read Gate was deactivated the drive requirement for Write Clocks to precede Write Gate by 250 ns would also be met.

Since the write driver turn on delay plus data encoder turn on delay is 6 Servo Clock periods maximum from the leading edge of Write Gate, the width of the Write Splice area recorded on the disk media will be 6 Servo Clock periods maximum.

PLO Sync Field Write

The PLO Sync field must consist of 11 valid and recoverable bytes of interface data zeros. From Figure 17 a 2-bit pad area is shown between the 6-bit splice area and the start of the data field PLO syunc. This 2-bit pad area allows the Read Gate to be enabled one bit minimum after a Write Splice and be valid at the Drive Interface prior to the Data Field PLO sync bytes. Thus, to guarantee writing 11 valid bytes of PLO Sync characters, allow for the Write Splice area, and allow Read Gate to be enabled one bit time after a Write Splice but prior to an 11-byte PLO Sync field, it is recommended that the Controller transmit 12 bytes of zeros after Write Gate is enabled for the Data field PLO Sync field.

Byte Sync, Data Field, ECC and Data Pad Write

After the Data Field PLO sync field is written a Byte Sync character should be written to enable the Controller to establish byte synchronization for the data field.

After the data field is written, the data field check codes should be written followed by one data pad byte at the end of the check field to ensure proper recording and recovery of the check field codes.

NOTE: In addition to these requirements an additional 1 byte end of record (EOR) field should be allowed for in the format design to account for tolerances between embedded servo areas.

After the data pad byte is written the Write Gate should be deactivated and Read Gate should not be activated to read the address Area of the next sector until 60 ±4 Servo Clock periods after the next Sector pulse is detected. This will allow ample time for the write-to-read recovery time (i.e., the 10 μs minimum between the trailing edge of Write Gate and the leading edge of Read Gate).

Summary of Critical Write Function Parameters

Controller timing variations in the record update function are allowed if the following drive dependent write (and interrelated read) timing parameters are met:

1. Read-To-Write Time

   Assuming head selection is stabilized, the time lapse from disabling Read Gate to enabling Write Gate shall be 3 Servo Clock periods minimum.

2. Write Clock-To-Write Time

   Write Clocks must precede Write Gate by a minimum of 250 ns

3. Write Driver plus Data Encoder Turn On From Write Gate

   The write driver plus data encoder turn on time (write splice width) is 6 servo clock periods maximum.

4. Write Driver Turn Off From Write Gate

   To account for data encoding delays, Write Gate must be held on for at least one byte time after the last bit of the information to be recorded. (see "Pad" in Figure 17).

5. Write-To-Read Recovery Time

   The time lapse before Read Gate can be enabled after disabling the Write Gate is 10 μs minimum.